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PEGATRON DT-MB RESTRICTED SECRET

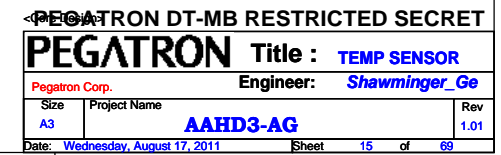
PEGATRON Title : DDR3 TERMINATION

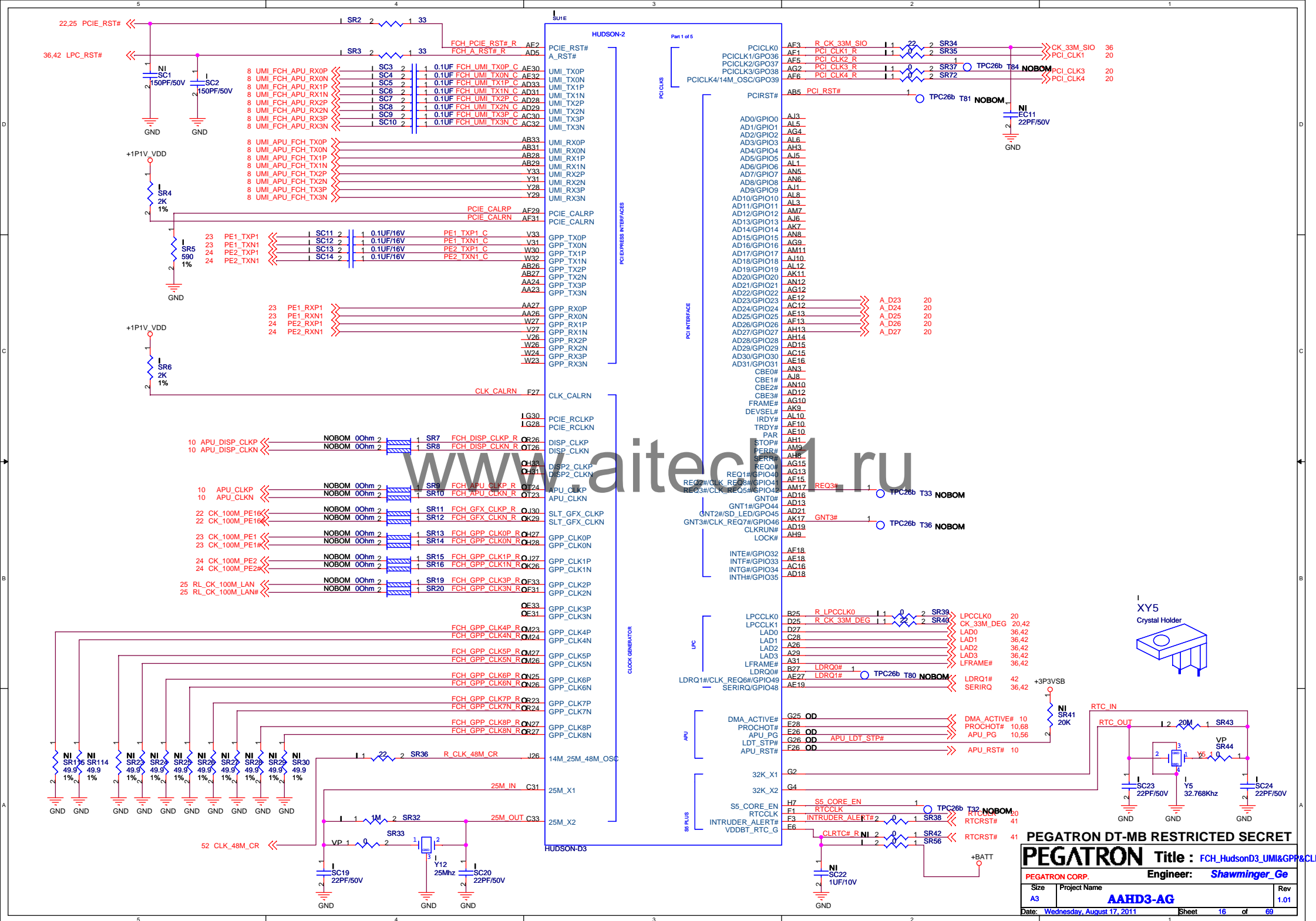
Pegatron Corp. Engineer: Shawminger_Ge

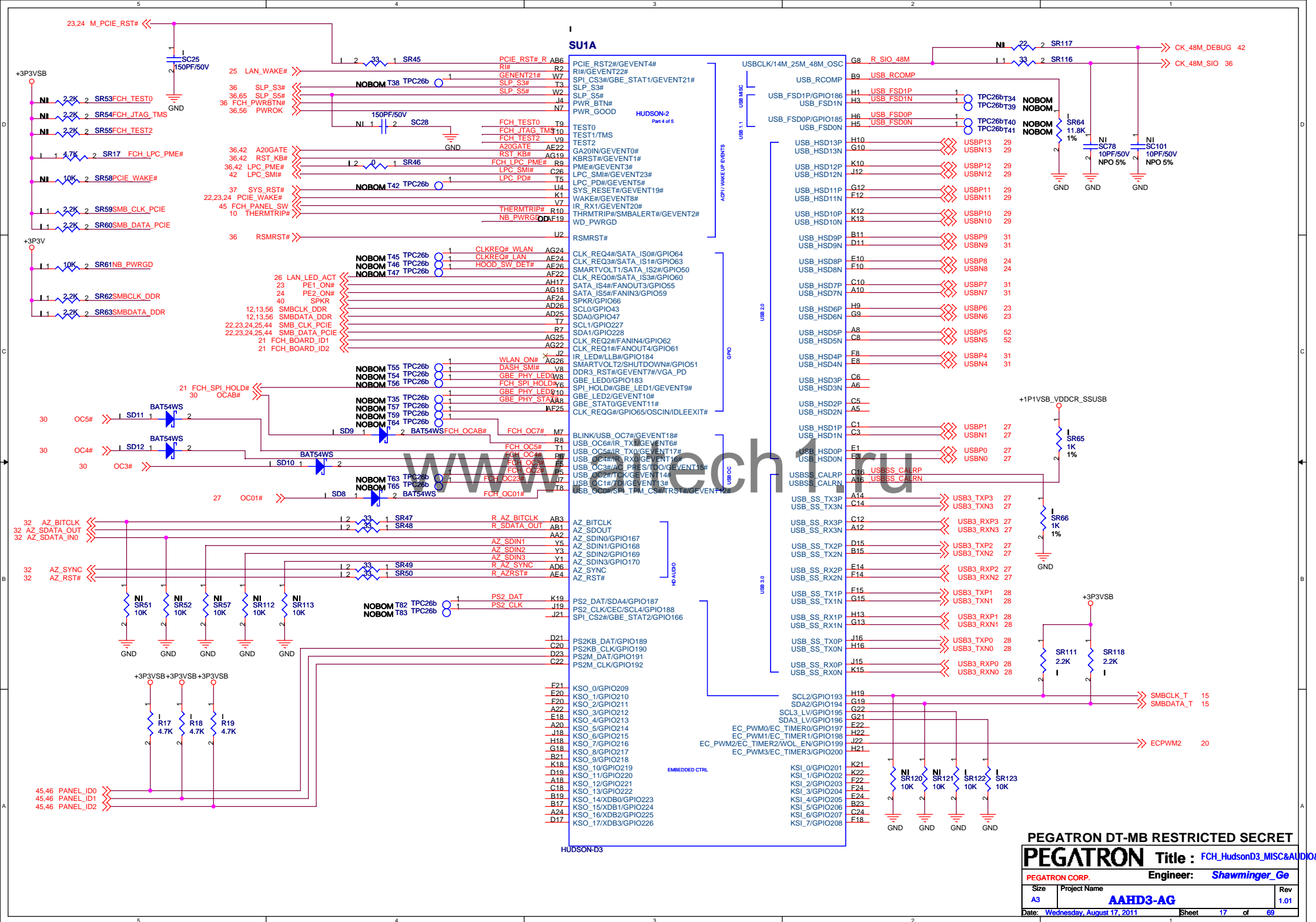
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|------------|--------------------------|-------------|
| Size A3 | Project Name AAHD3-AG | Rev 1.01 |
|------------|--------------------------|-------------|

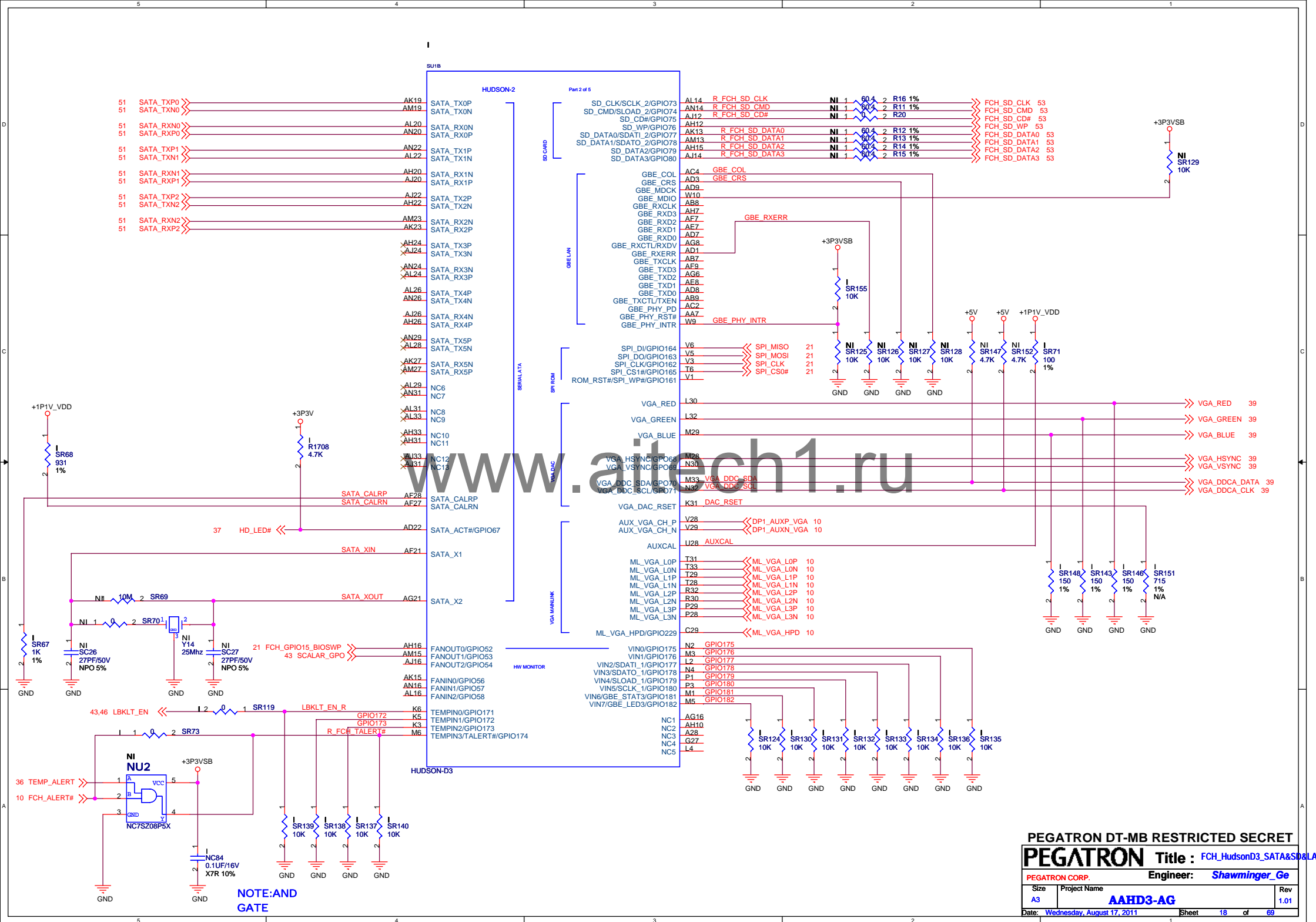
Date: Wednesday, August 17, 2011 Sheet 14 of 69

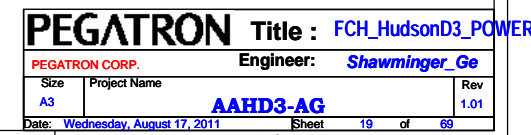
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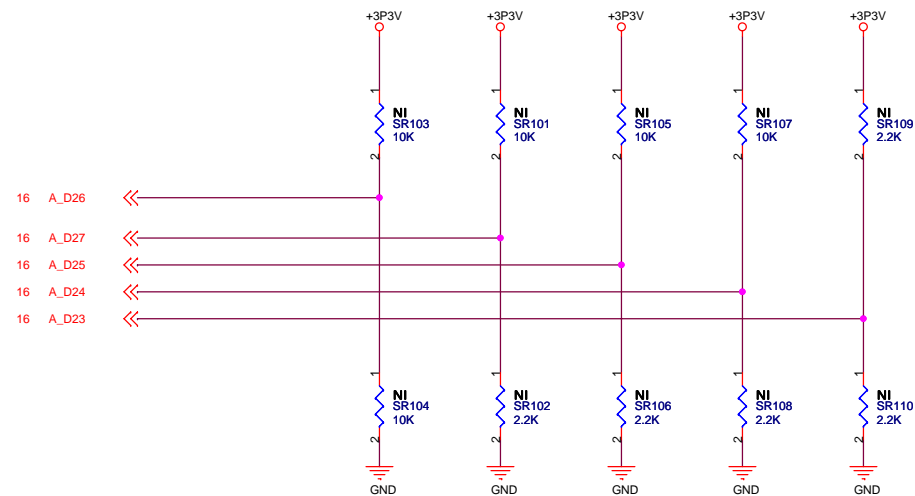
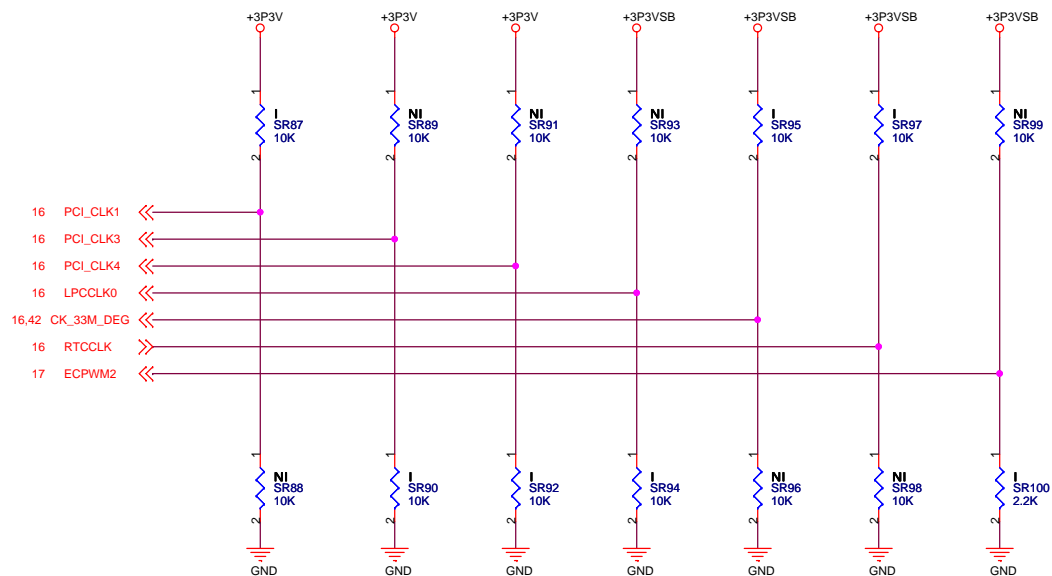






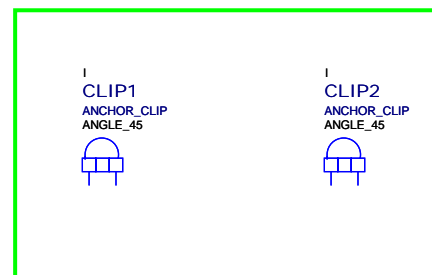
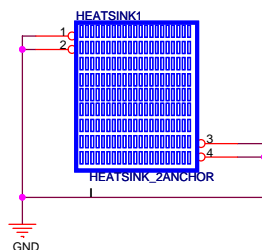






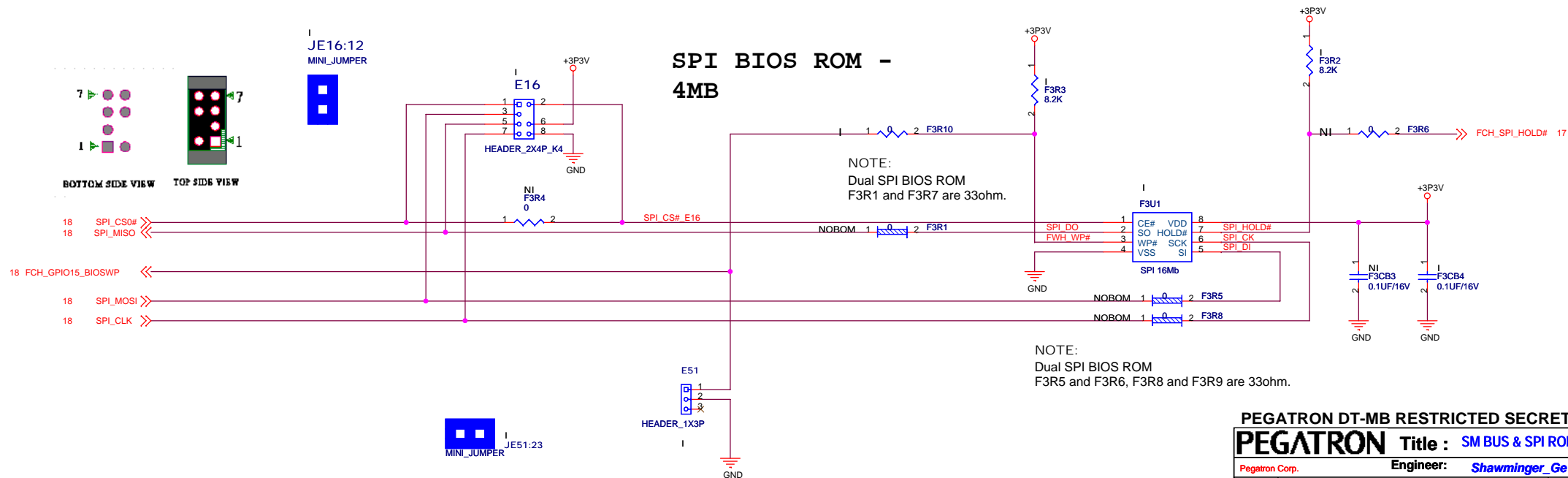
| | EC_PWM2 ECPWM2 | LPCCLK0 LPCCLK0 | LPCCLK1 CK_33M_DEG | PCICLK1 PCI_CLK1 | PCICLK3 PCI_CLK3 | PCICLK4 PCI_CLK4 | RTCCLK RTCCLK |
|-------------|-------------------|--------------------|----------------------------------|---------------------|---------------------|------------------------------|------------------|
| Pull High 1 | LPC ROM | ENABLE IMC | ENABLE INTERNAL CLOCK GENERATOR | ALLOW PCIE GEN2 | ENABLE DEBUG MODE | INTER CLOCK REQUIRED SETTING | DISABLE S5+ MODE |
| Pull low 0 | SPI ROM | DISABLE IMC | DISABLE INTERNAL CLOCK GENERATOR | FORCE PCIE GEN2 | DISABLE DEBUG MODE | RESERVED | ENABLE S5+ MODE |

AAHD3-AG 1.01 Add





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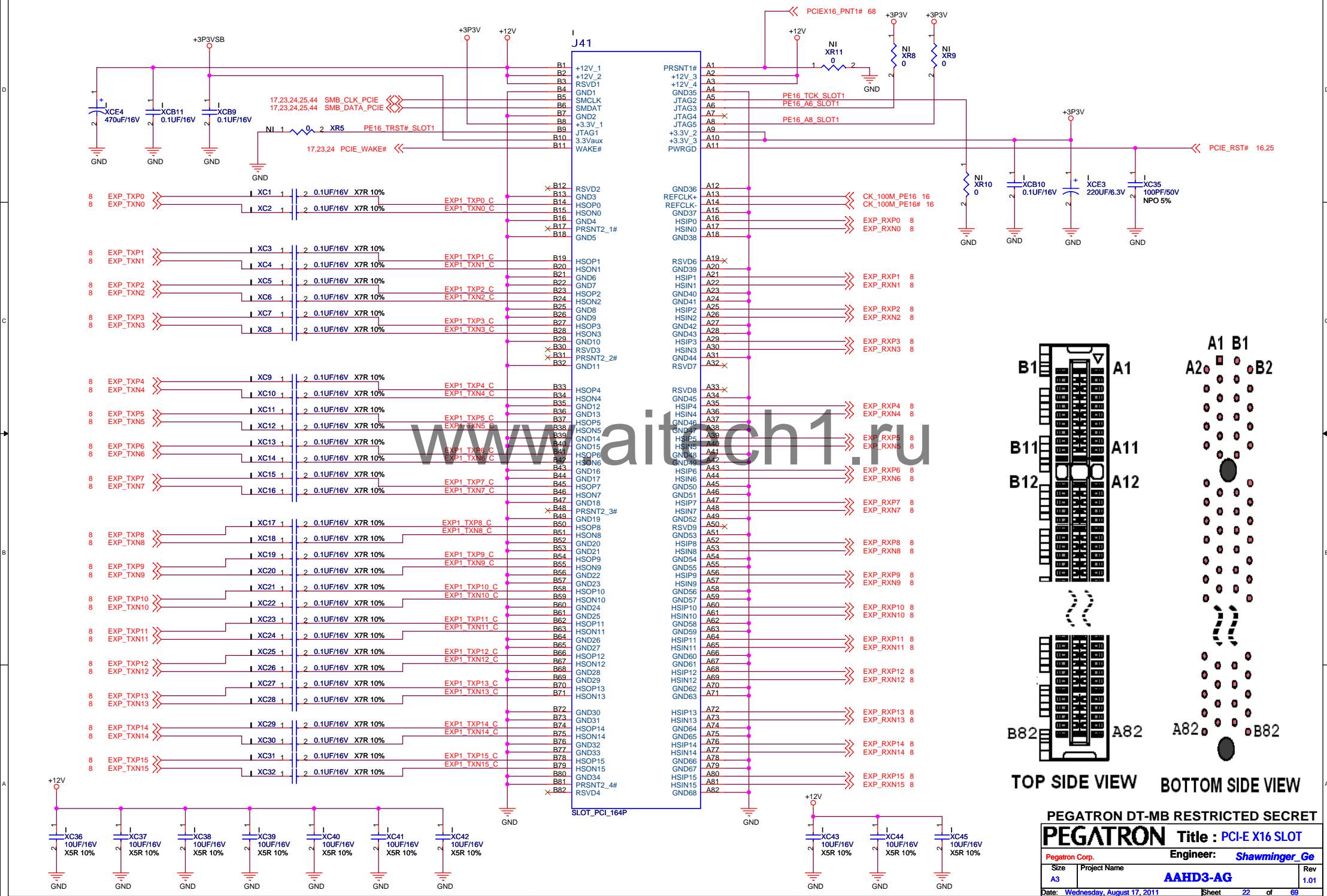
PEGATRON Title : SM BUS & SPI ROM

Pegatron Corp. Engineer: Shawminger_Ge

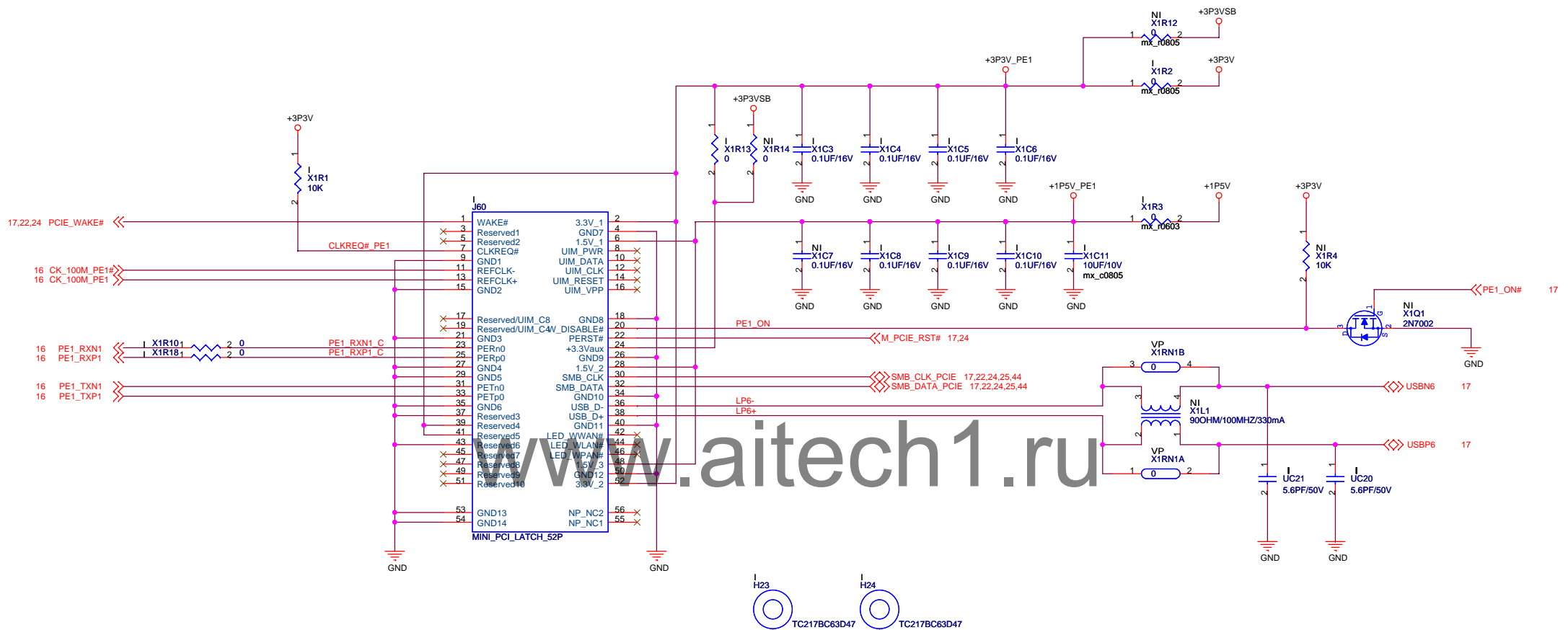
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|------------|--------------------------|-------------|
| Size A3 | Project Name AAHD3-AG | Rev 1.01 |
|------------|--------------------------|-------------|

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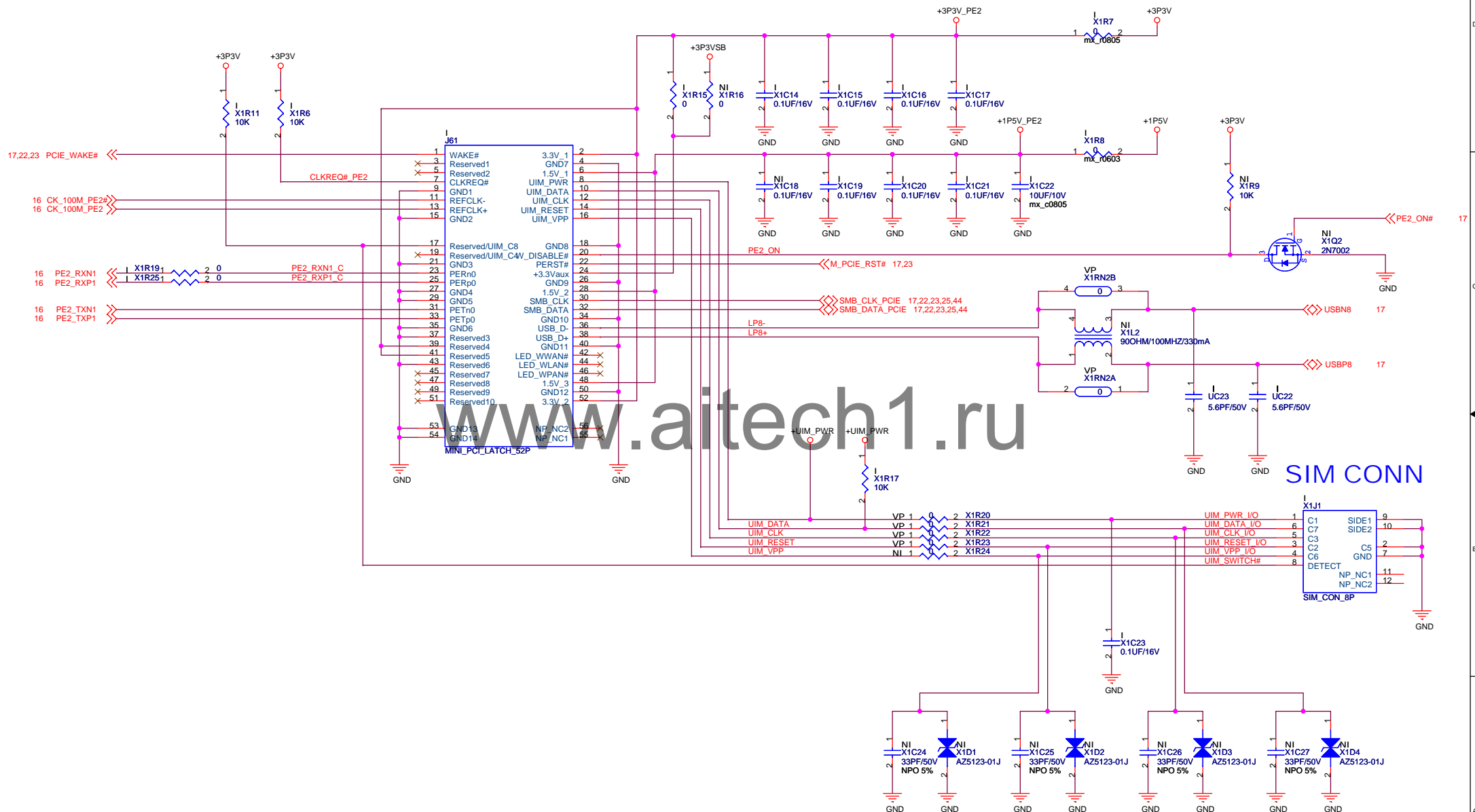
PCI EXPRESS X16 Graphics Card Slot



Mini-PCIE Slot (Half Card) for Wifi



Mini-PCIE Slot (Full Card)



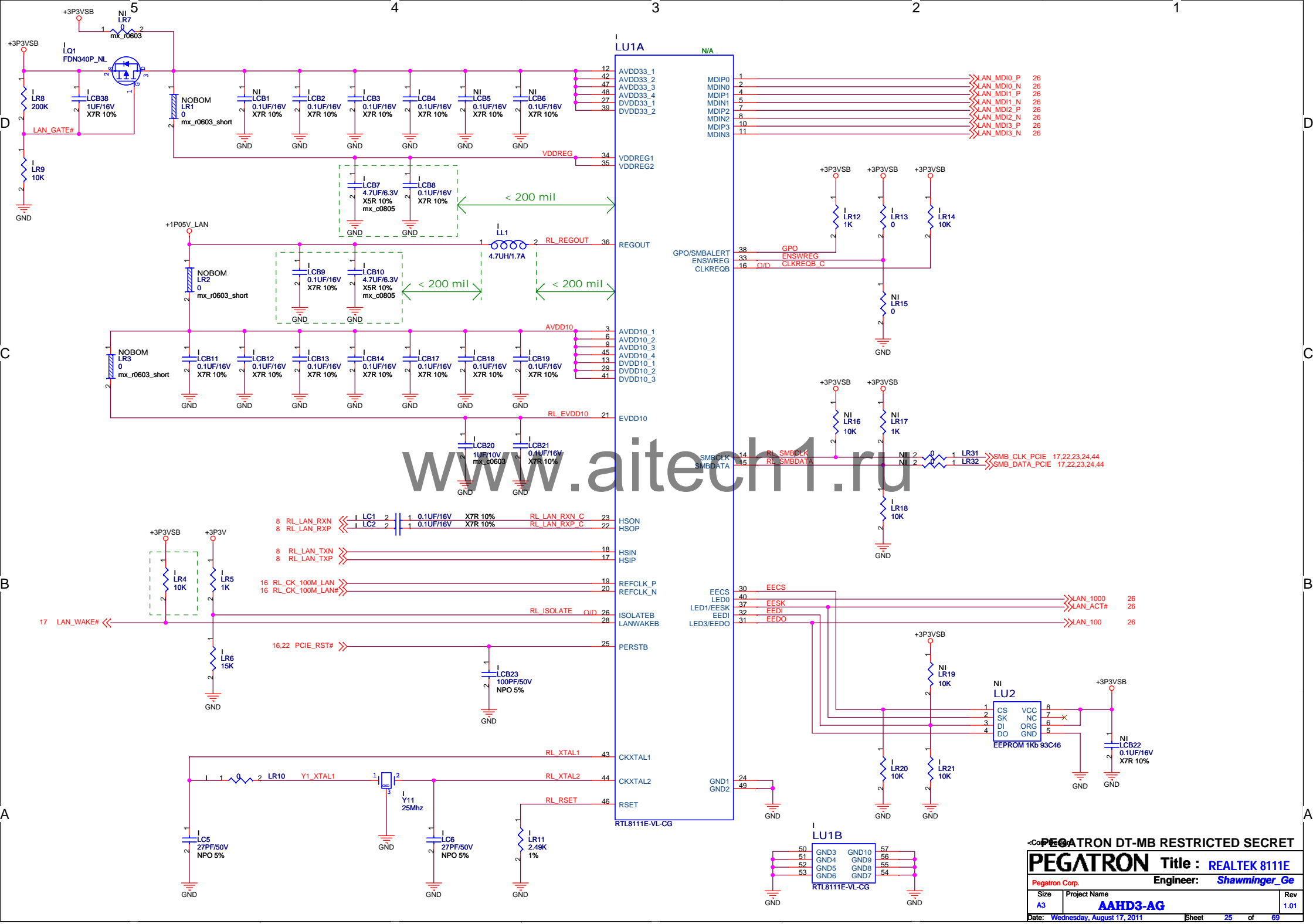
PEGATRON DT-MB RESTRICTED SECRET

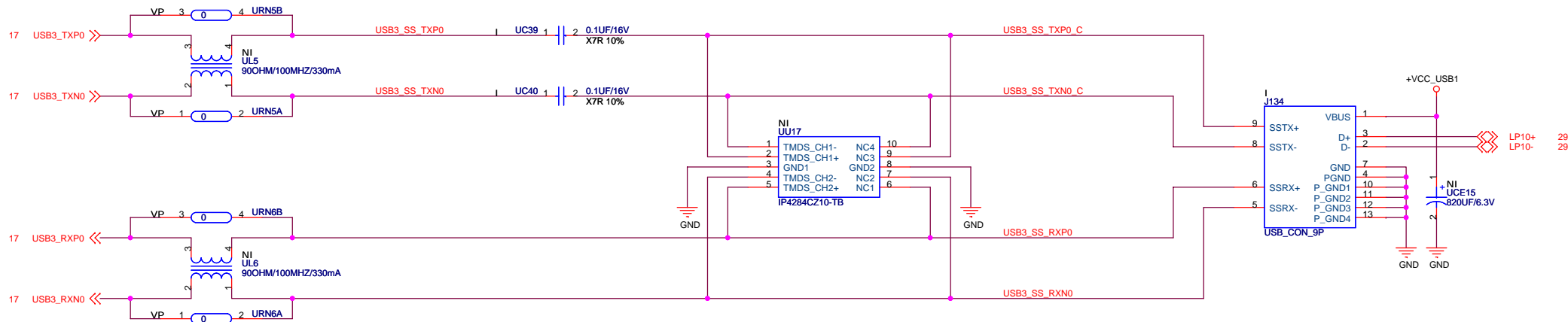
PEGATRON Title : MINI-PCIE SLOT-2

Pegatron Corp. Engineer: Shawminger_Ge

| | | |
|------------|---------------------------------|-------------|
| Size A3 | Project Name AAHD3-AG | Rev 1.01 |
|------------|---------------------------------|-------------|

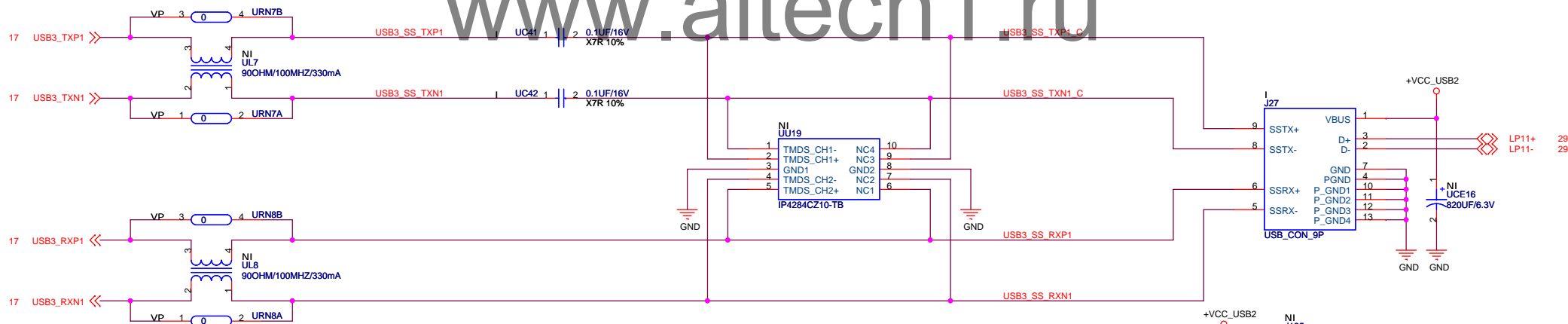
Date: Wednesday, August 17, 2011 Sheet 24 of 69





1213-00LN000 USB2.0

| PIN NO. | 1 | 2 | 3 | 4 |
|-------------|--------------------|----|----|------|
| SIGNAL NAME | VBUS | D- | D+ | PGND |
| REMARK | USB2.0 CONTACT PIN | | | |



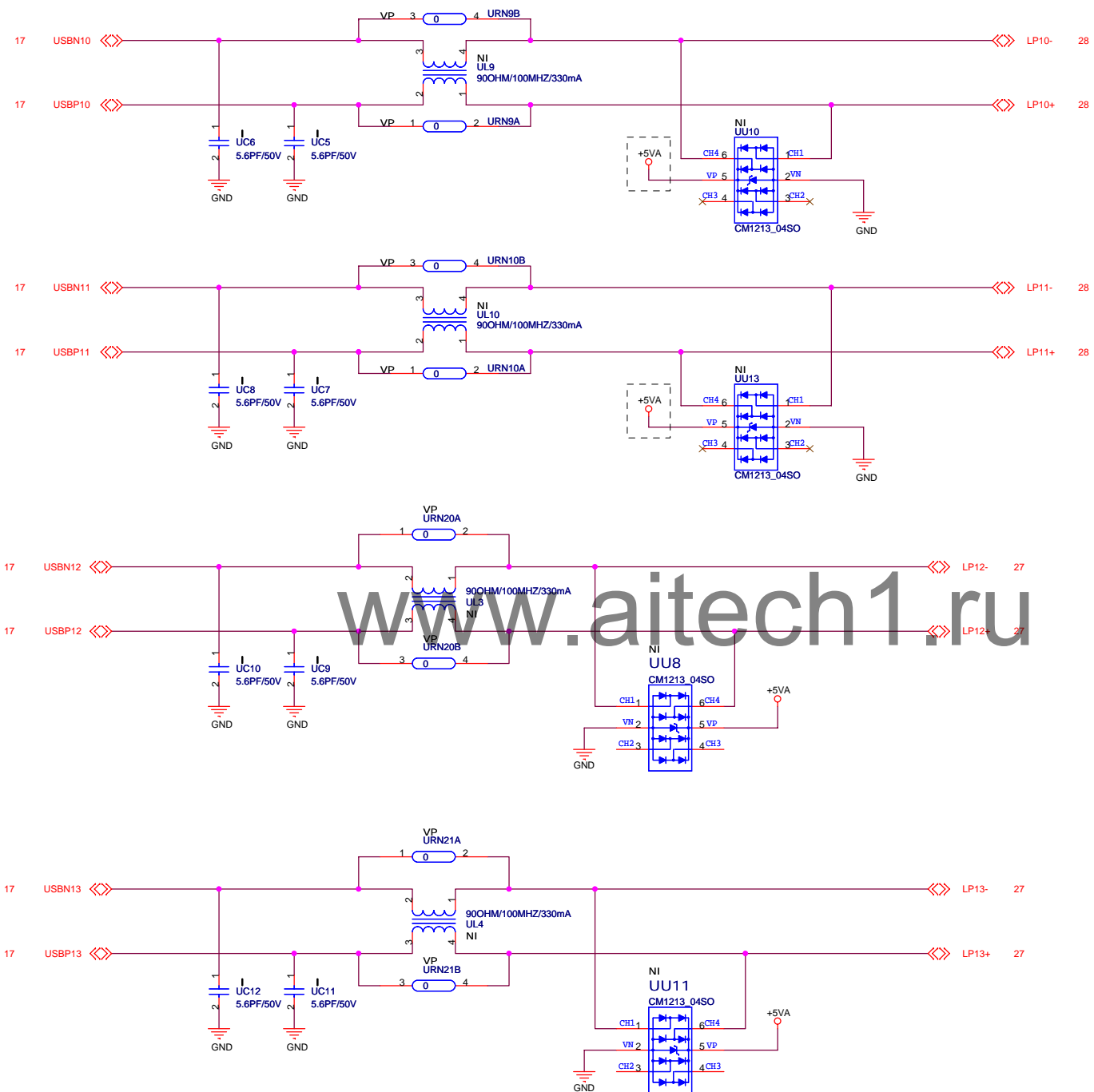
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SIDE USB3.0 PORT

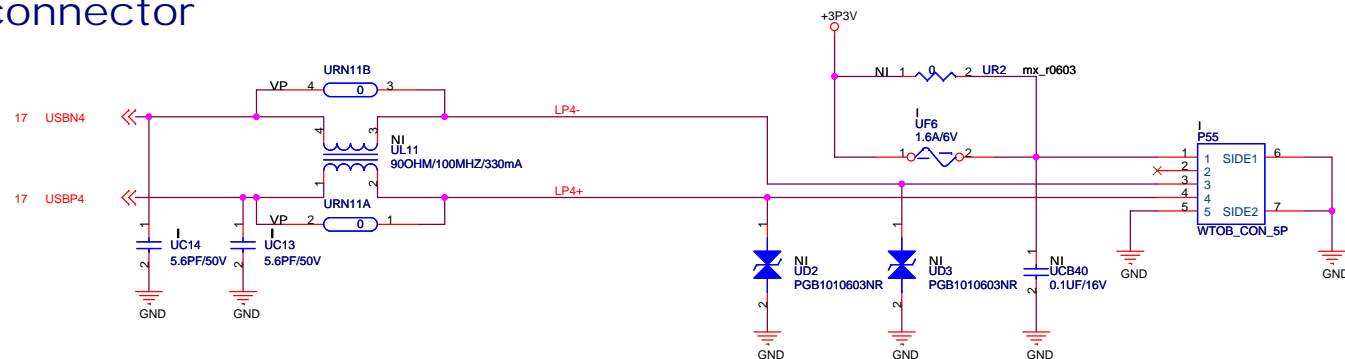
Pegatron Corp. Engineer: Shawminger_Ge

Size A3 Project Name AAHD3-AG Rev 1.01

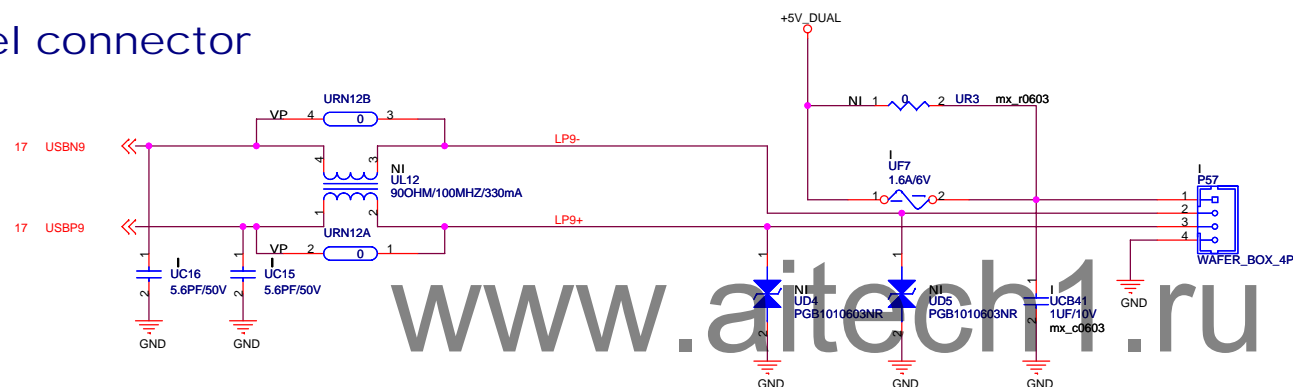
Date: Wednesday, August 17, 2011 Sheet 28 of 69



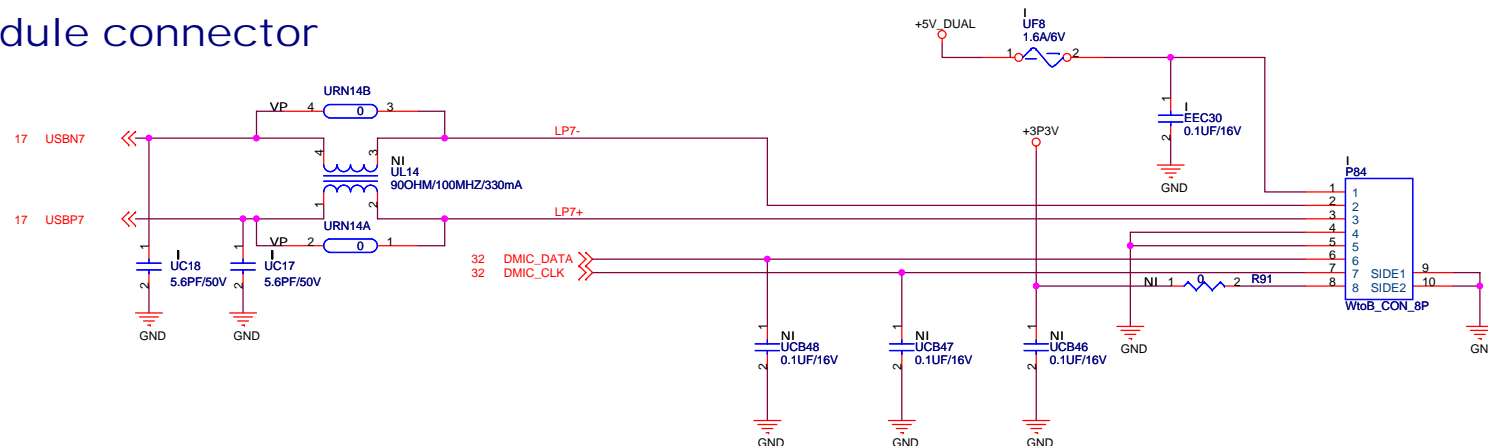
Touch Panel connector



Touch Panel connector

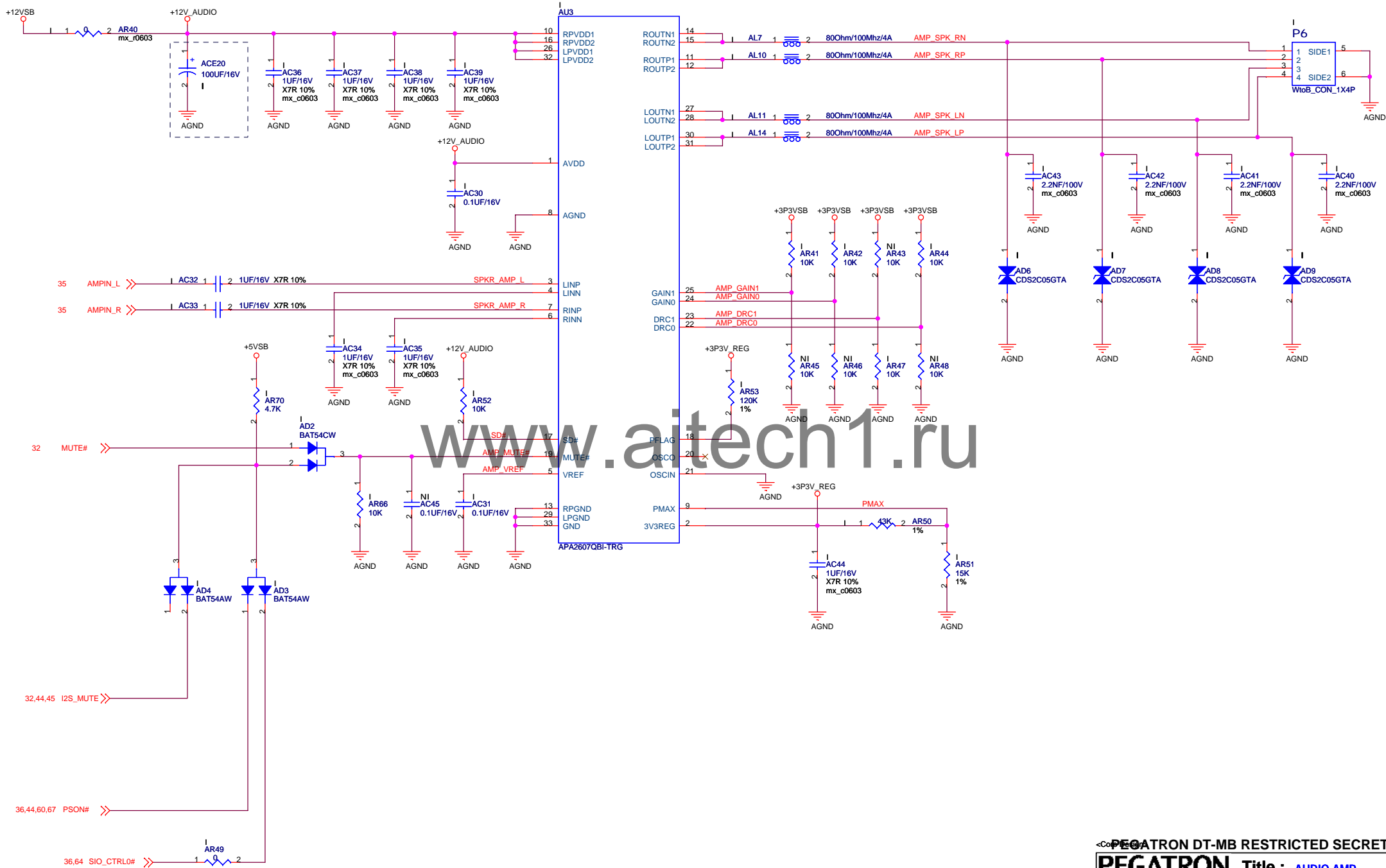


Camera Module connector

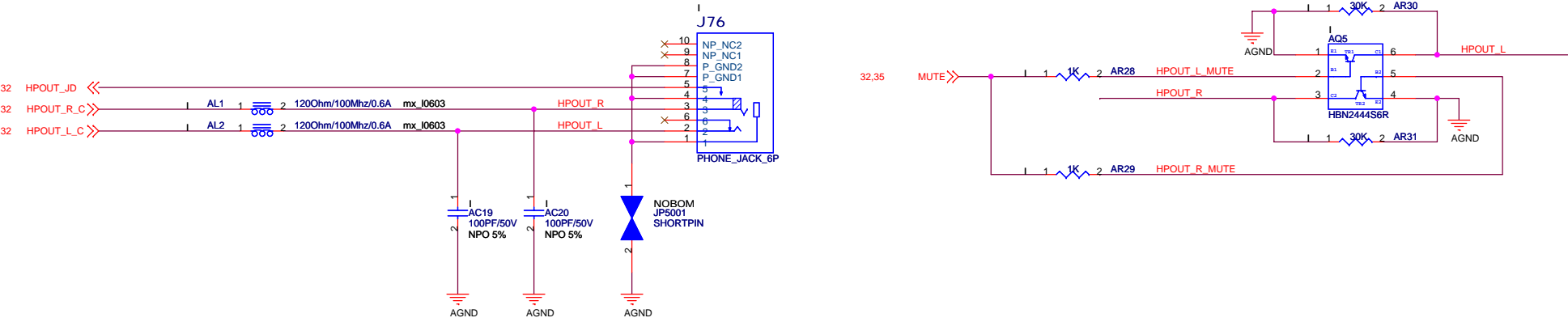


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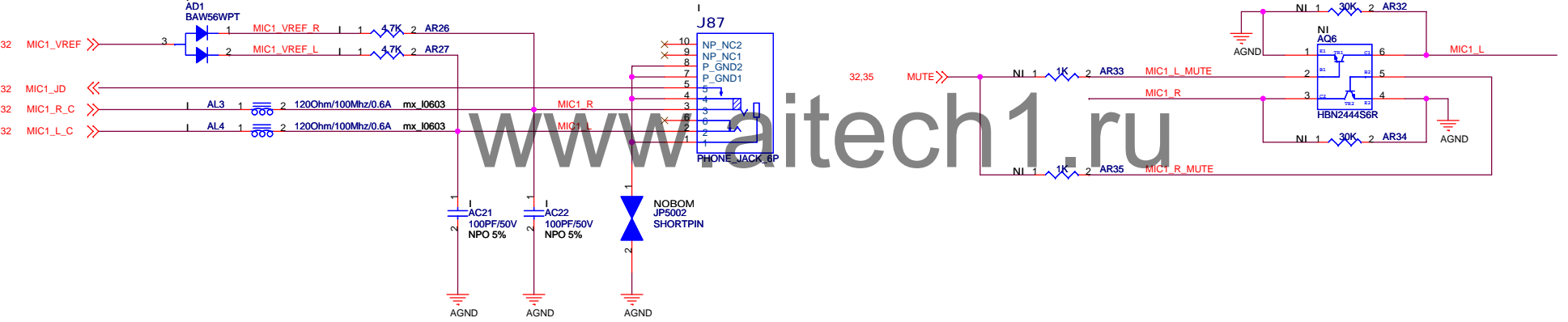




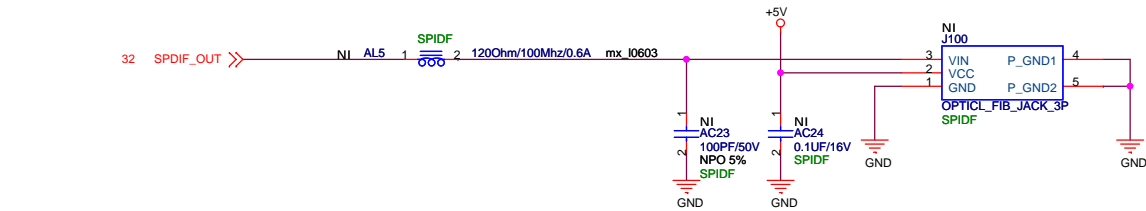
HEADPHONE



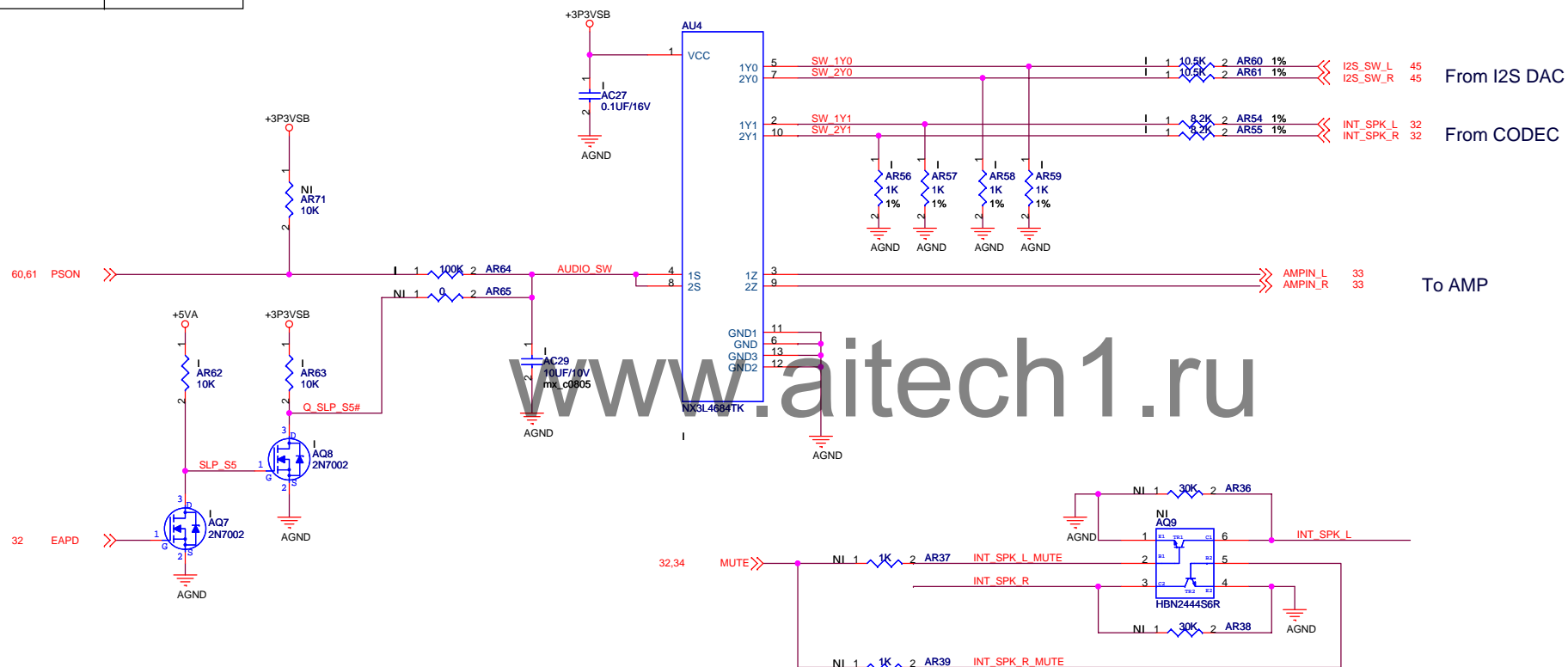
MIC

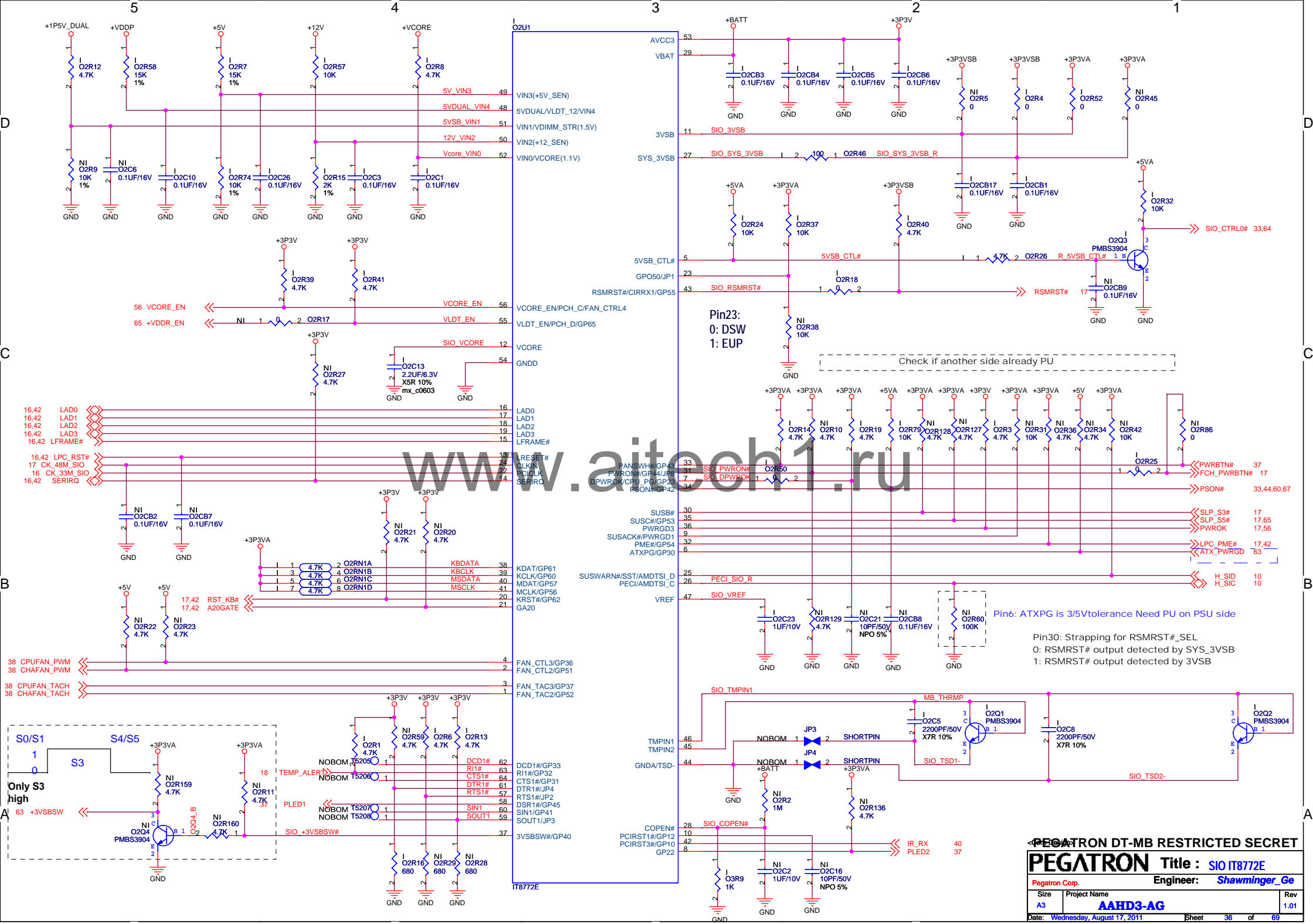


SPDIF OUT

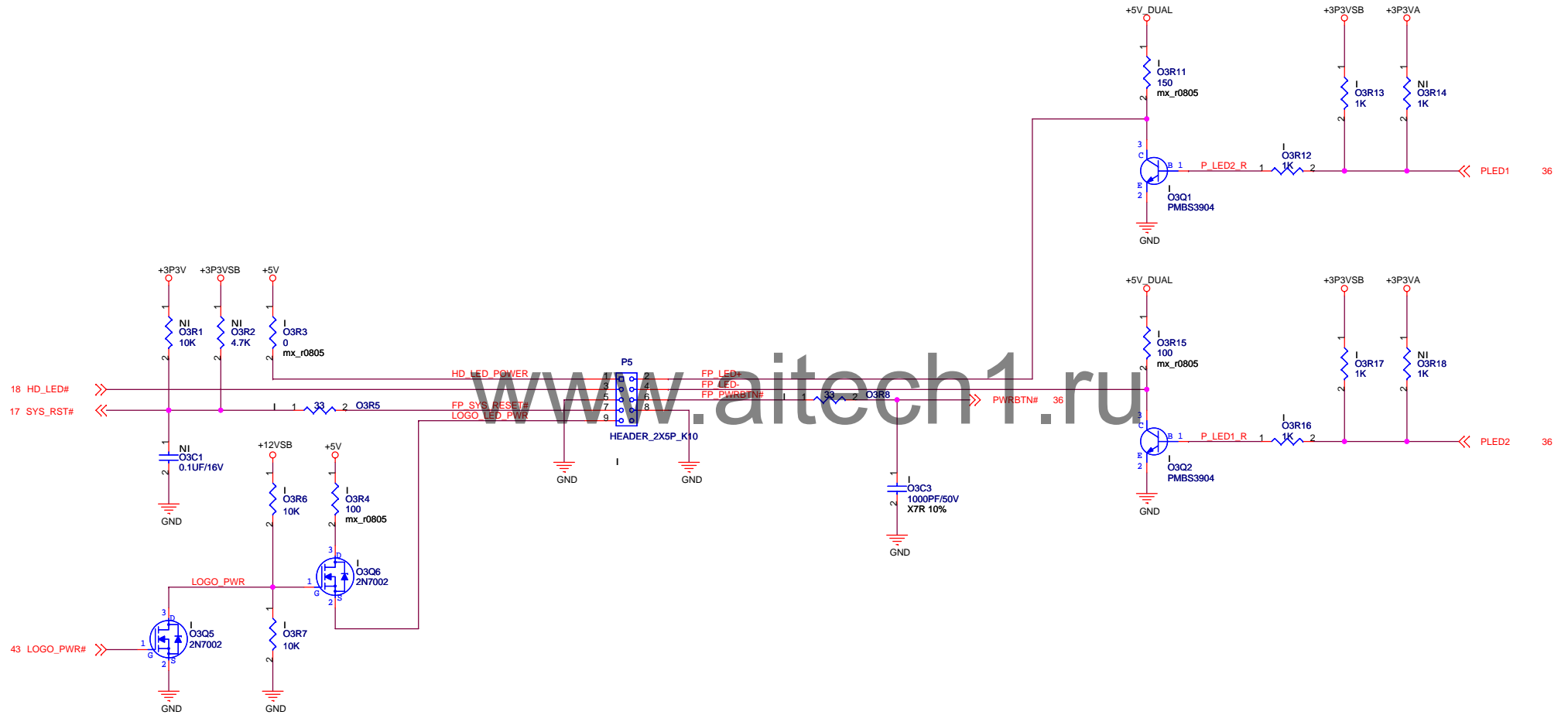


| | |
|----------|--------|
| AUDIO_SW | OUTPUT |
| L | Y0 |
| H | Y1 |





FRONT PANEL / LED CIRCUITRY



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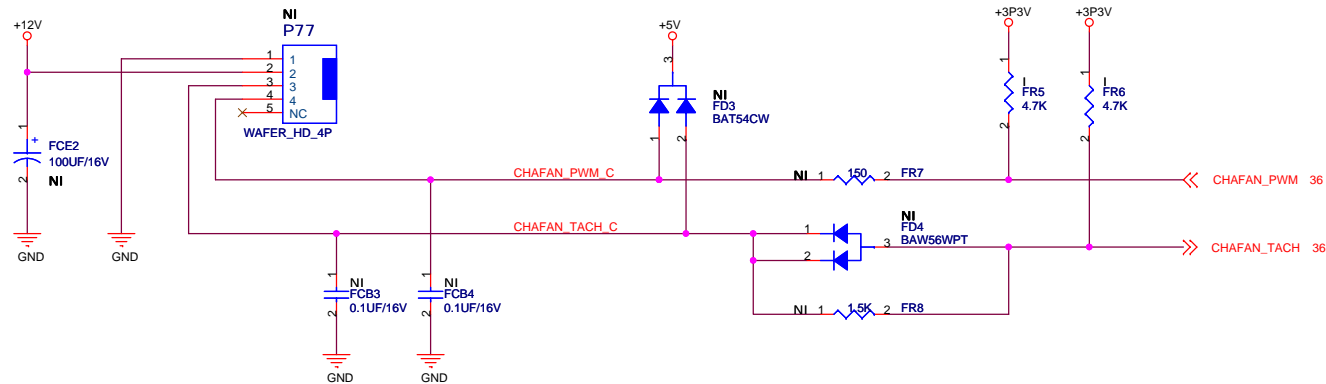
PEGATRON Title : FRONT PANEL

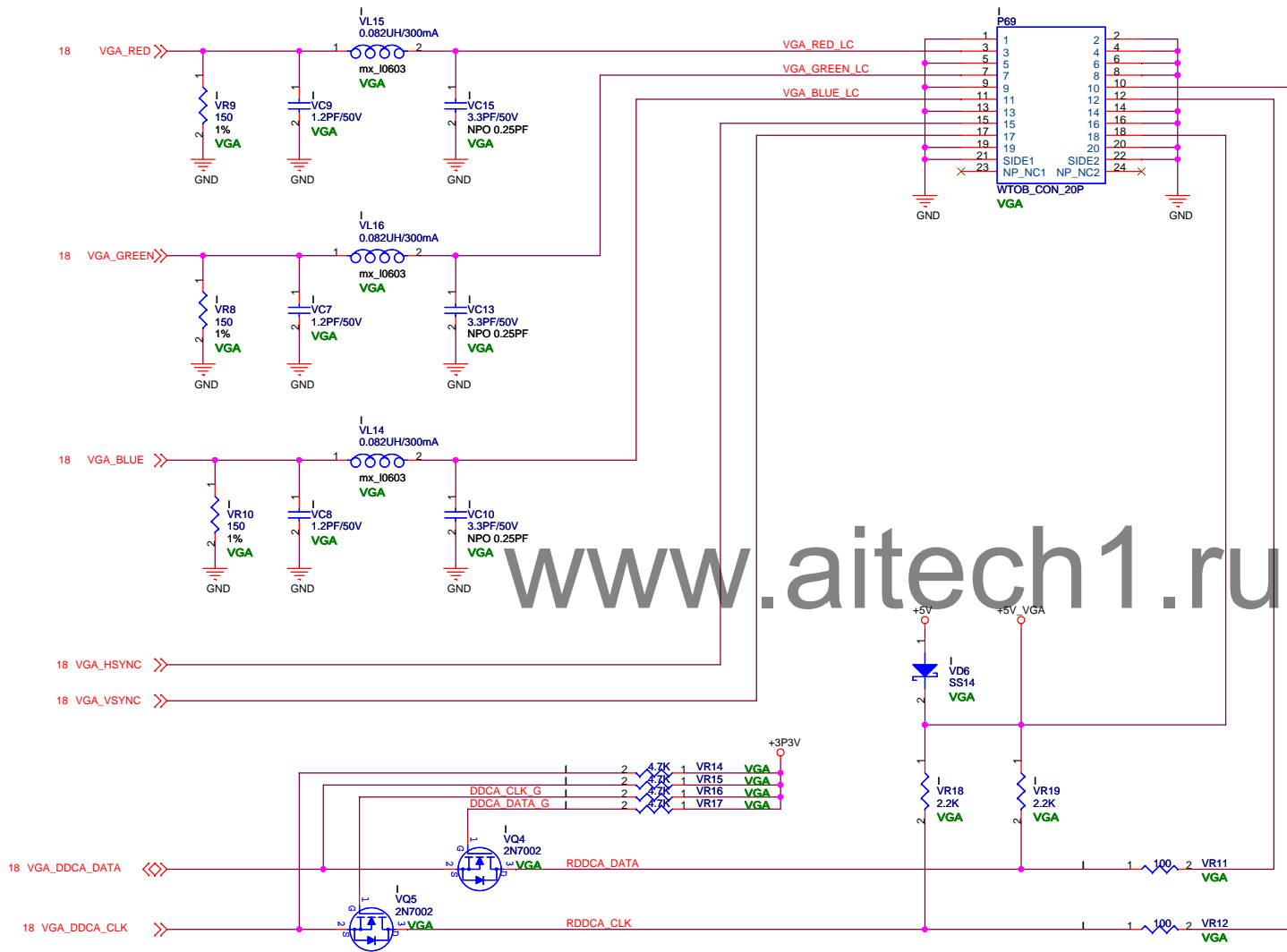
Pegatron Corp. Engineer: Shawminger_Ge

| Size | Project Name | Rev |
|------|--------------|------|
| A3 | AAHD3-AG | 1.01 |

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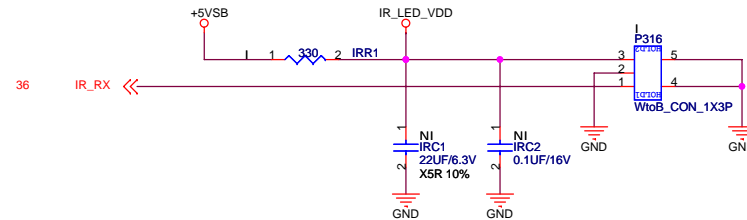
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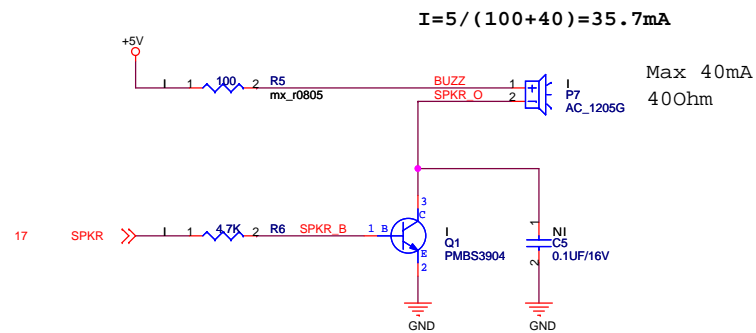
www.aitech1.ru

IR LED

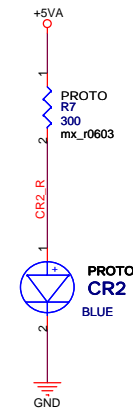


www.aitech1.ru

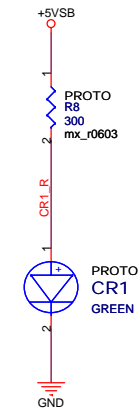
SPEAKER



+5VA : BLUE

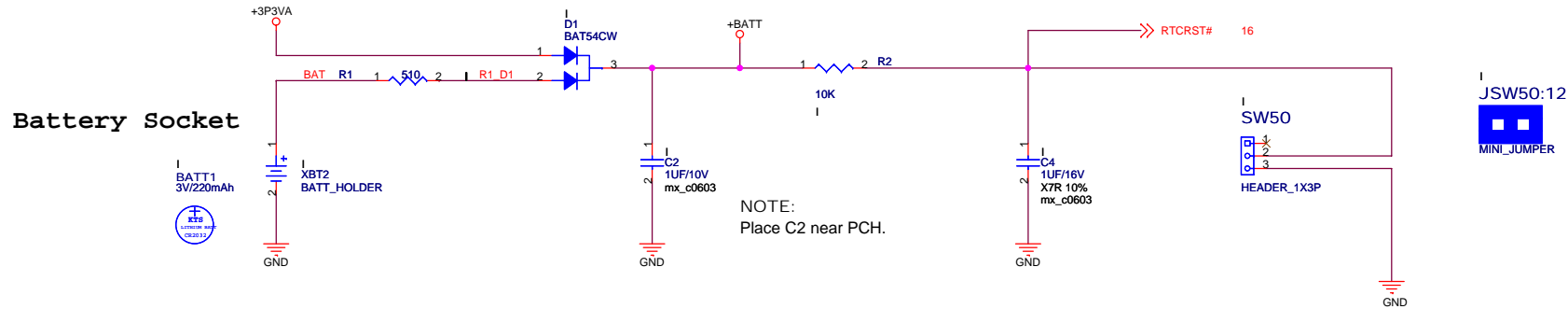


+5VSB : GREEN

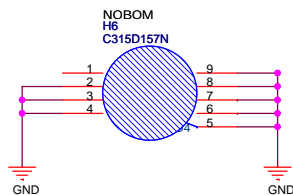
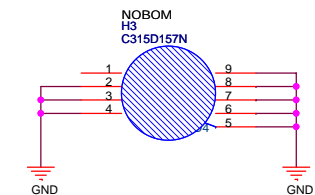
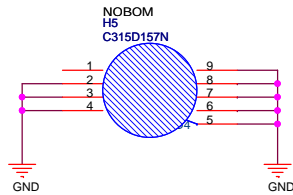
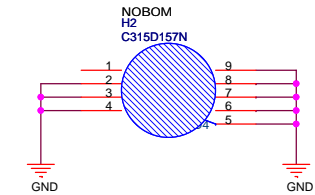
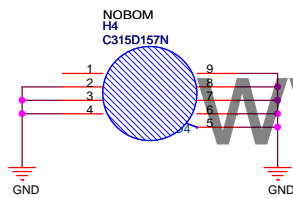
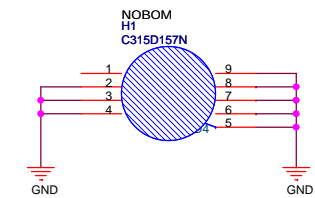


External RTC Circuitry

CLEAR CMOS



| RTC DATA | |
|----------|---------|
| 1-2 | Default |
| 2-3 | CLEAR |

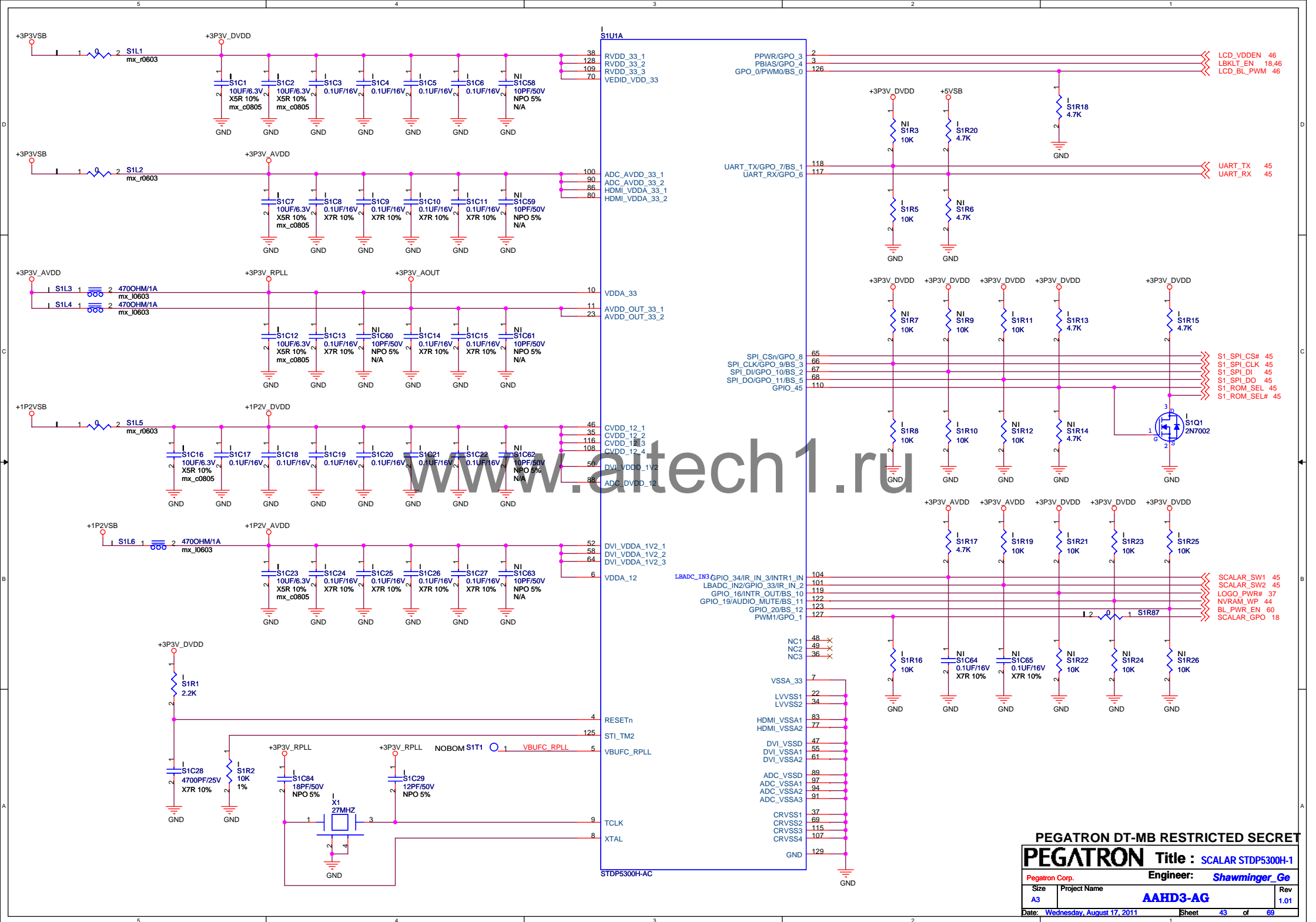


Pinout diagram for the PROTO P12 header:

- Pin 1: +3P3V
- Pin 2: GND
- Pin 3: CK_33M_DEG
- Pin 4: LPC_RST#
- Pin 5: LAD0
- Pin 6: LAD1
- Pin 7: LAD2
- Pin 8: LFRAME#
- Pin 9: GND
- Pin 10: GND
- Pin 11: GND
- Pin 12: GND
- Pin 13: GND
- Pin 14: GND

The diagram illustrates the pin connections for the NI GP1 module. The module has a 24-pin header (NI GP1) with pins numbered 1 to 24. The connections are as follows:

- Power Connections:**
 - +3P3VA, +3P3V, +5VA, +5V, +12V, and +BATT are connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, and 23 respectively.
- Signal Connections:**
 - CK_33M_DEG (pins 16, 20) is connected to pin 2.
 - LFRAME# (pin 16, 36) is connected to pin 4.
 - LPC_RST# (pin 16, 36) is connected to pin 6.
 - LAD3 (pin 16, 36) is connected to pin 8.
 - LAD1 (pin 16, 36) is connected to pin 10.
 - LPC_SMI# (pin 17) is connected to pin 12.
 - A20GATE (pin 17, 36) is connected to pin 14.
 - RST_KB# (pin 17, 36) is connected to pin 16.
 - LAD2 (pin 16, 36) is connected to pin 18.
 - LAD0 (pin 16, 36) is connected to pin 20.
 - SERIRQ (pin 16, 36) is connected to pin 22.
 - CK_48M_DEBUG (pin 17) is connected to pin 24.
 - LDRQ1# (pin 16) is connected to pin 2.
 - LPC_PME# (pin 17, 36) is connected to pin 4.
- Ground Connections:**
 - Two GND pins are shown at the bottom, connected to pins 1 and 24.



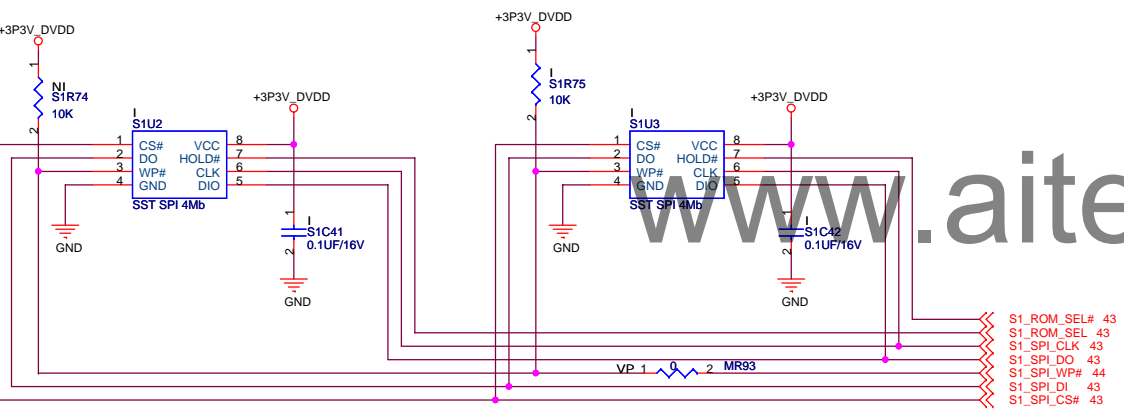
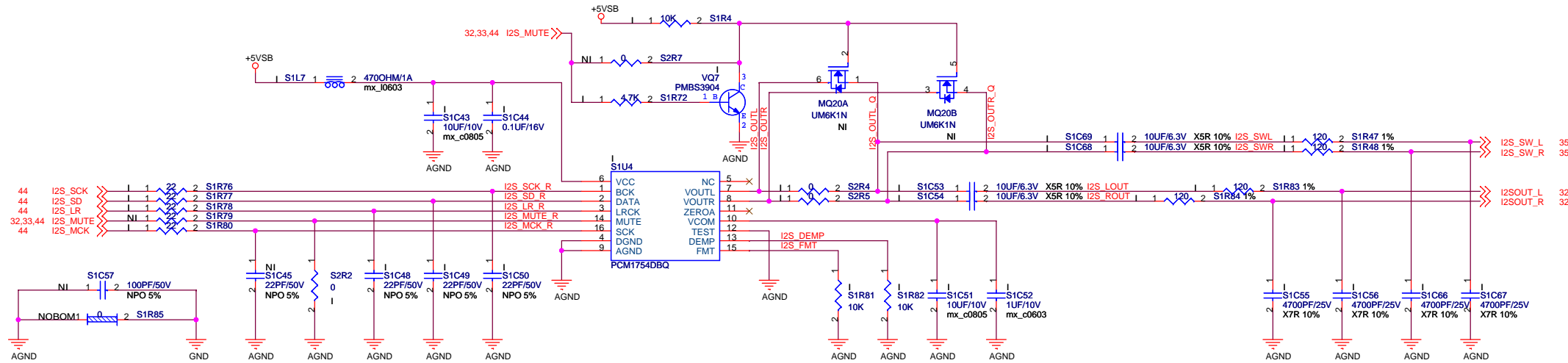
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SCALAR STDP5300H-1

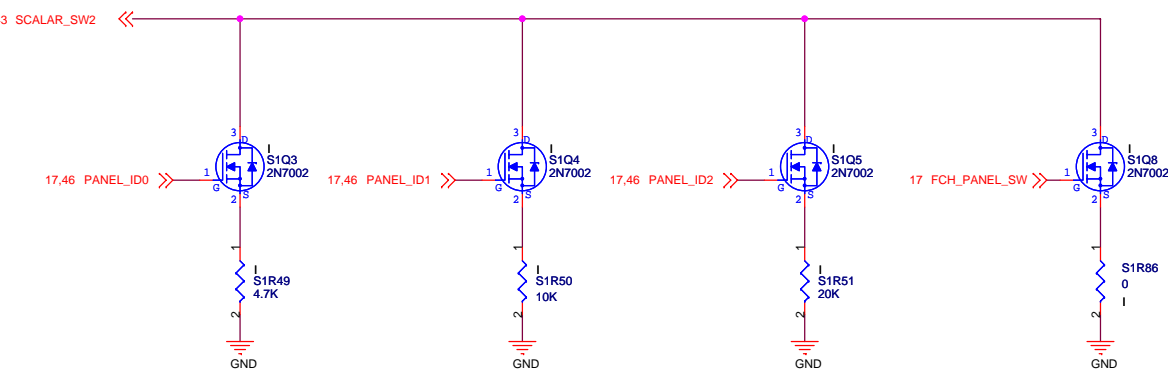
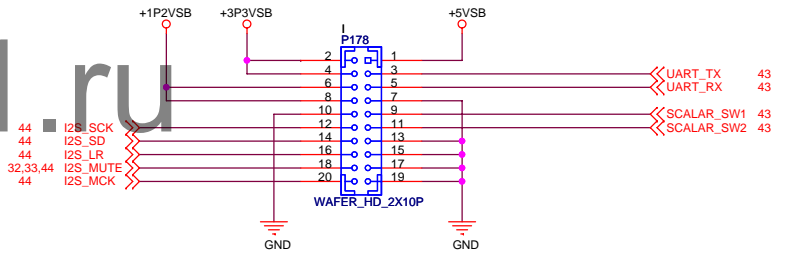
Pegatron Corp. Engineer: Shawminger_Ge

Size A3 Project Name AAHD3-AG Rev 1.01

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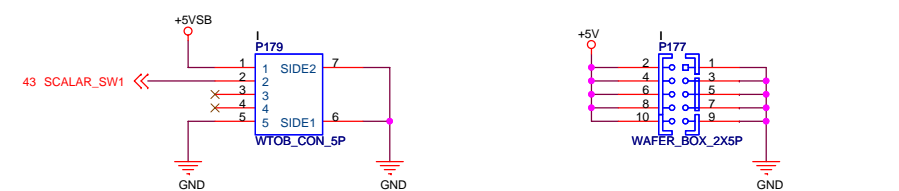


3D Scaler



KEYPAD

3D PANEL



AAHD3-AG 1.02A Change for LCD_PWM Issue

CONVERTER

The circuit diagram shows a DC-DC converter. The input is +19V_BL_F, which passes through a 0.1µF/25V capacitor (VC6) and a 10k resistor (VR7) to the non-inverting input of the op-amp (P175). The op-amp's output drives the gate of the MOSFET (NI VQ8 2N7002). The MOSFET's source is connected to ground, and its drain is connected to the positive terminal of the load. The load consists of a 10k resistor (VR20), a 10k resistor (VR21), and a 10k resistor (VR22) in parallel. The negative terminal of the load is connected to ground. A diode (NI SD13) is connected between the MOSFET's drain and the positive terminal of the load. A 10k resistor (VR23) is connected between the MOSFET's gate and the positive terminal of the load. A 10k resistor (VR24) is connected between the MOSFET's gate and ground.

Legend:

- PANEL_ID0 17,45
- PANEL_ID1 17,45
- PANEL_ID2 17,45
- LCD_BL_PWM 43
- LBKLT_EN 18,43

The schematic shows a component labeled 'P176' with two pins. Pin 1 is connected to a +12V DC source, and Pin 2 is connected to a common ground (GND). The component is also labeled 'WAFER_BOX_2P'.

FROM CARD

49 DVI_TXP0_DIS
49 DVI_TXN0_DIS
49 DVI_TXP1_DIS
49 DVI_TXN1_DIS
49 DVI_TXP2_DIS
49 DVI_TXN2_DIS
49 DVI_CLKP_DIS
49 DVI_CLKN_DIS

49 DVI_CLK_DIS
49 DVI_DATA_DIS

49 DVI_HPD_DIS

FROM APU

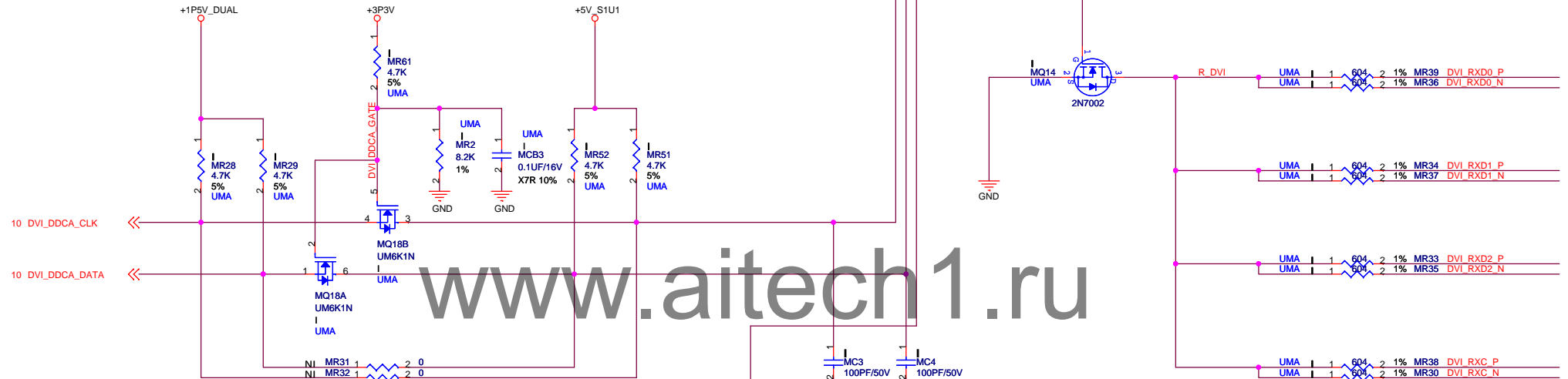
10 DVI_TMDSB_DATA0
10 DVI_TMDSB_DATA0#
10 DVI_TMDSB_DATA1
10 DVI_TMDSB_DATA1#
10 DVI_TMDSB_DATA2
10 DVI_TMDSB_DATA2#
10 DVI_TMDSB_CLK
10 DVI_TMDSB_CLK#

TO SCALER

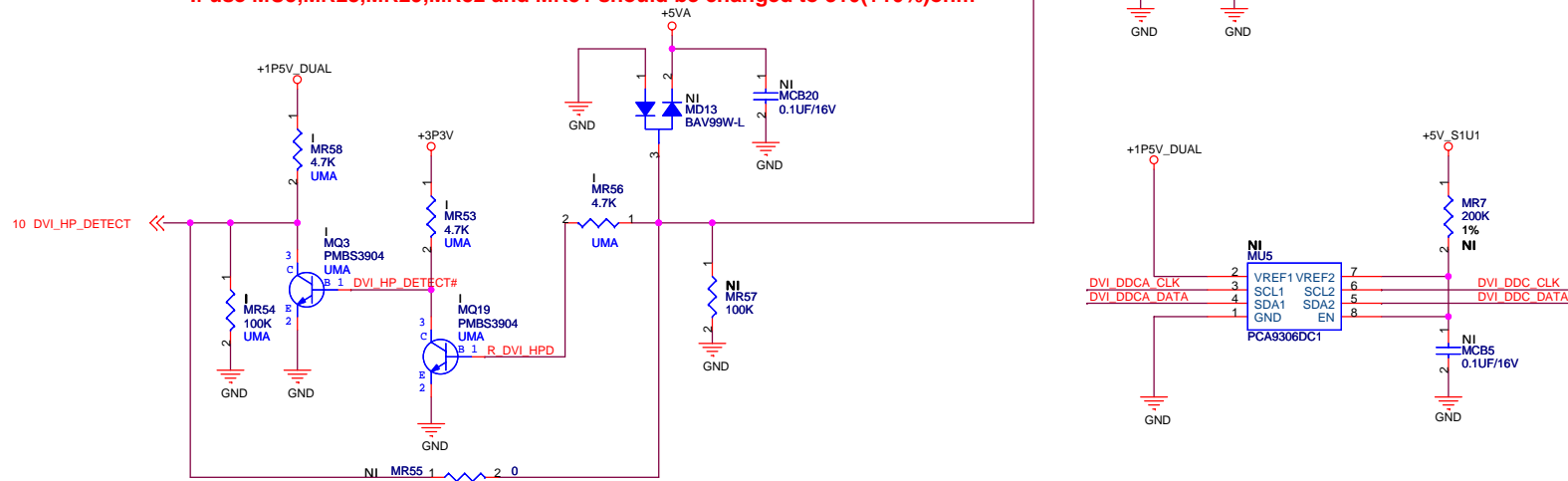
DVI_RXD0_P 44
DVI_RXD0_N 44
DVI_RXD1_P 44
DVI_RXD1_N 44
DVI_RXD2_P 44
DVI_RXD2_N 44
DVI_RXC_P 44
DVI_RXC_N 44

DVI_DDC_CLK 44
DVI_DDC_DATA 44

DVI_HPD 44



If use MU5,MR28,MR29,MR52 and MR51 should be changed to 310(+10%)ohm

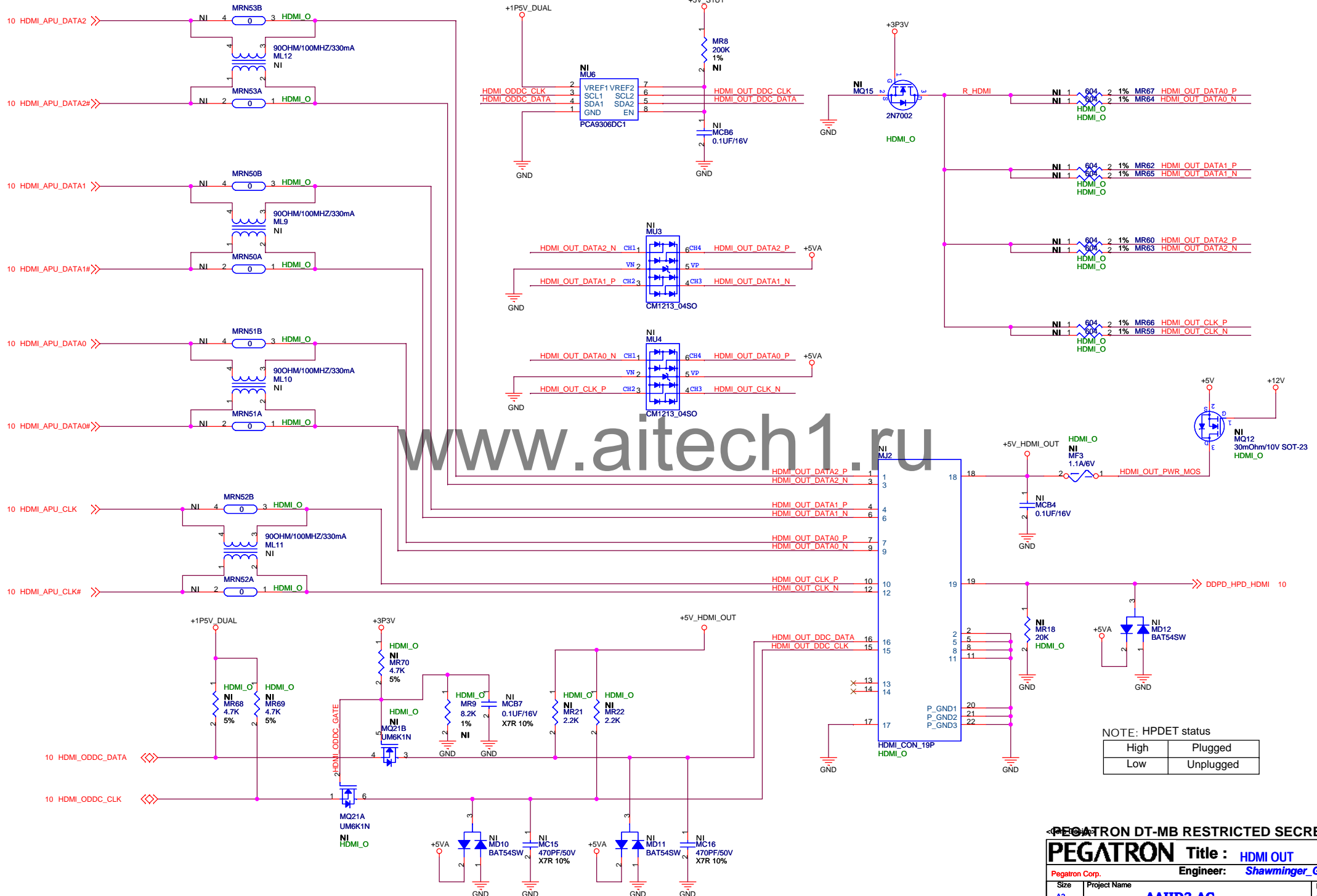


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PEGATRON Title : **DVI MUX**
Pegatron Corp. Engineer: **Shawminger_Ge**

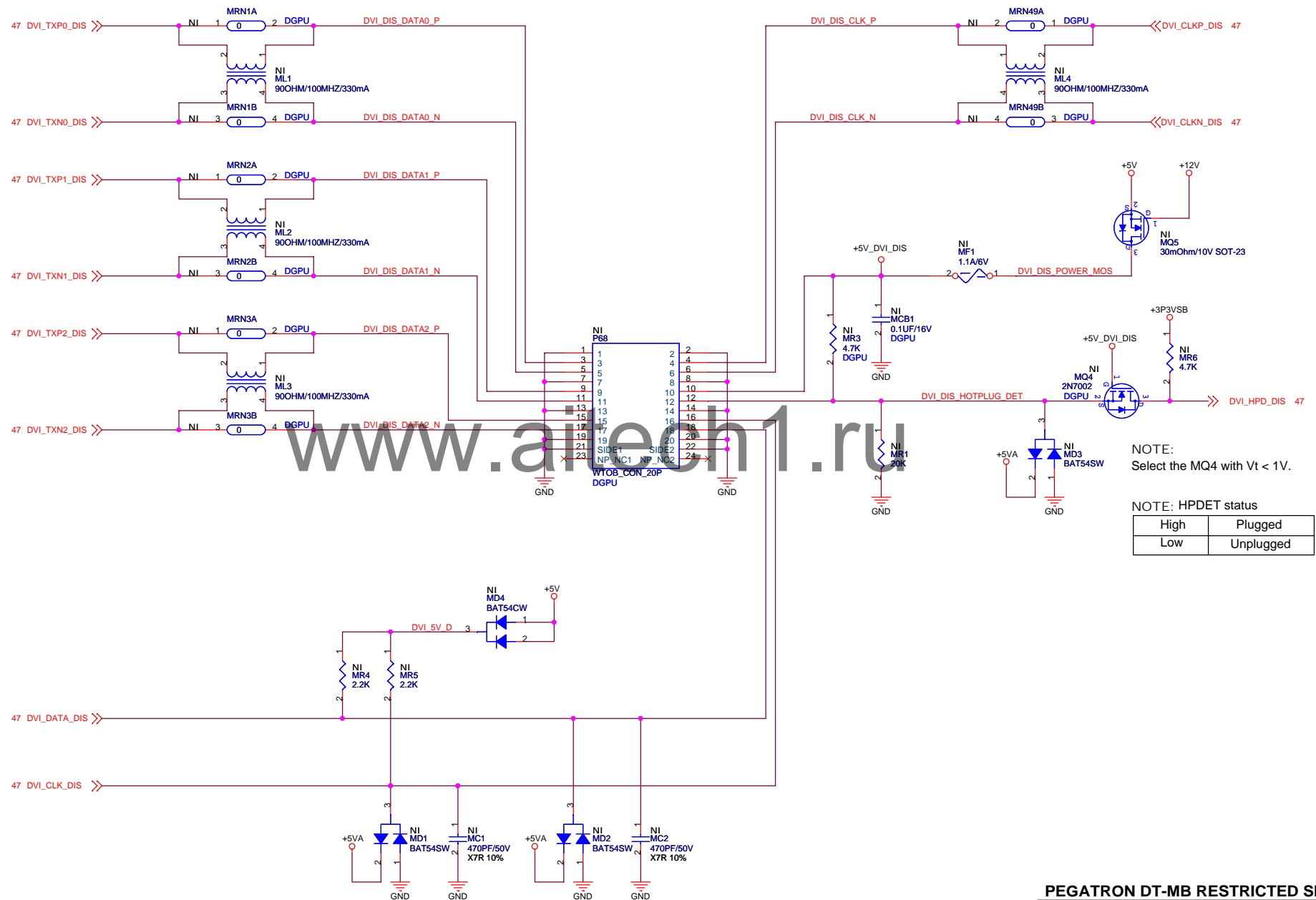
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| Size A3 | Project Name AAHD3-AG | Rev 1.01 |
| Date: Wednesday, August 17, 2011 | Sheet 47 of 69 | |

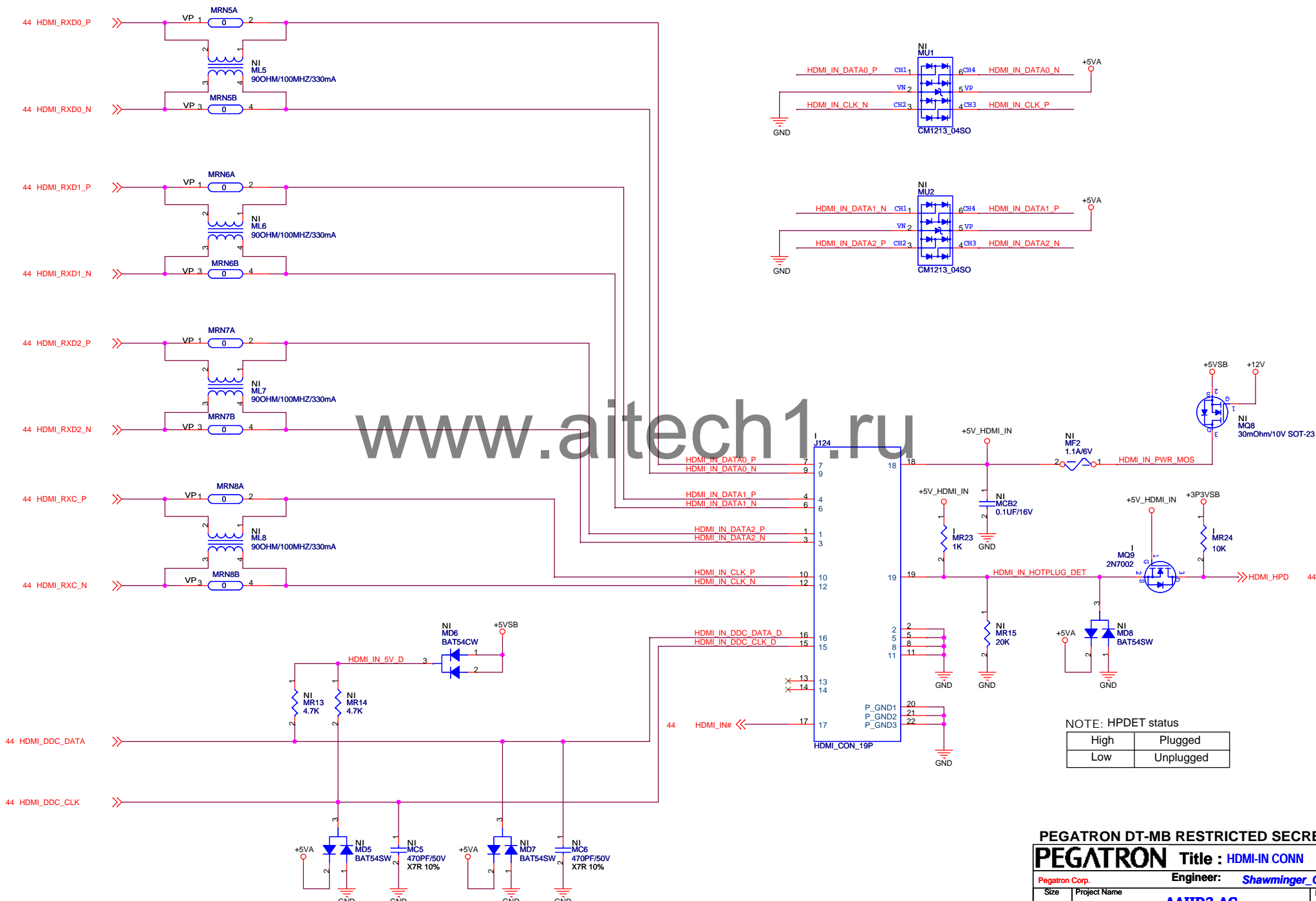
NOTE:
Place those AC Caps near to HDMI connector.



NOTE: HPDET status

| | |
|------|-----------|
| High | Plugged |
| Low | Unplugged |

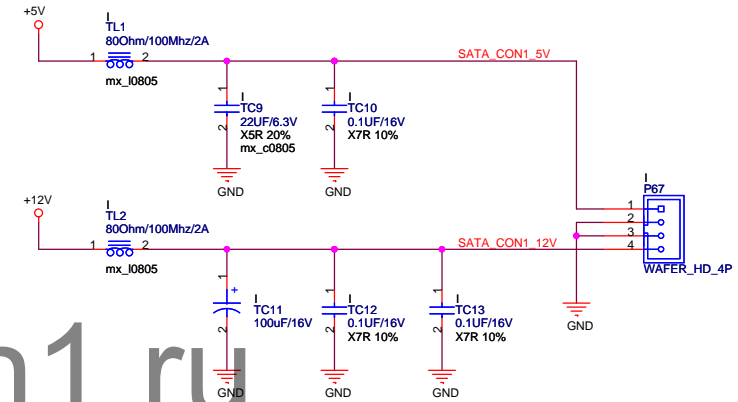
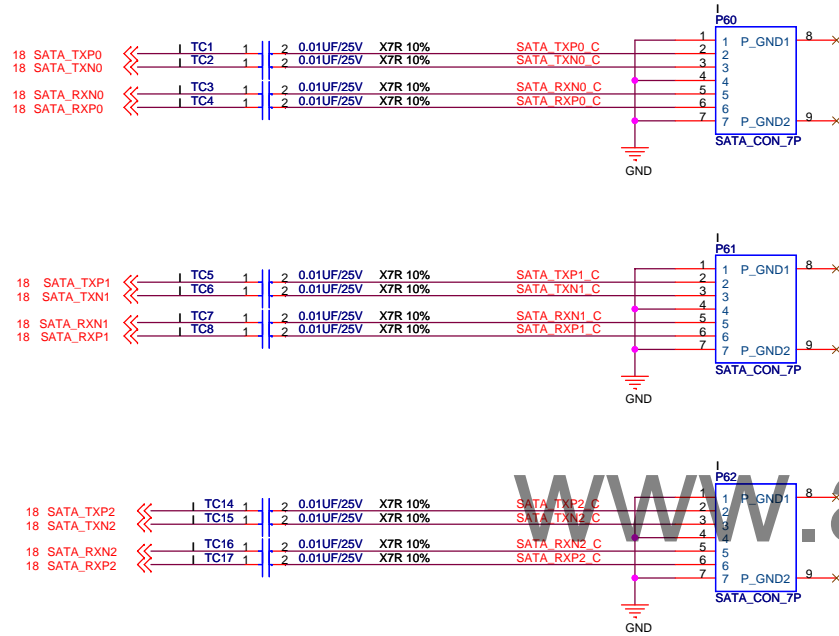




NOTE: HPDET status

| | |
|------|-----------|
| High | Plugged |
| Low | Unplugged |

SATA CONNECTOR



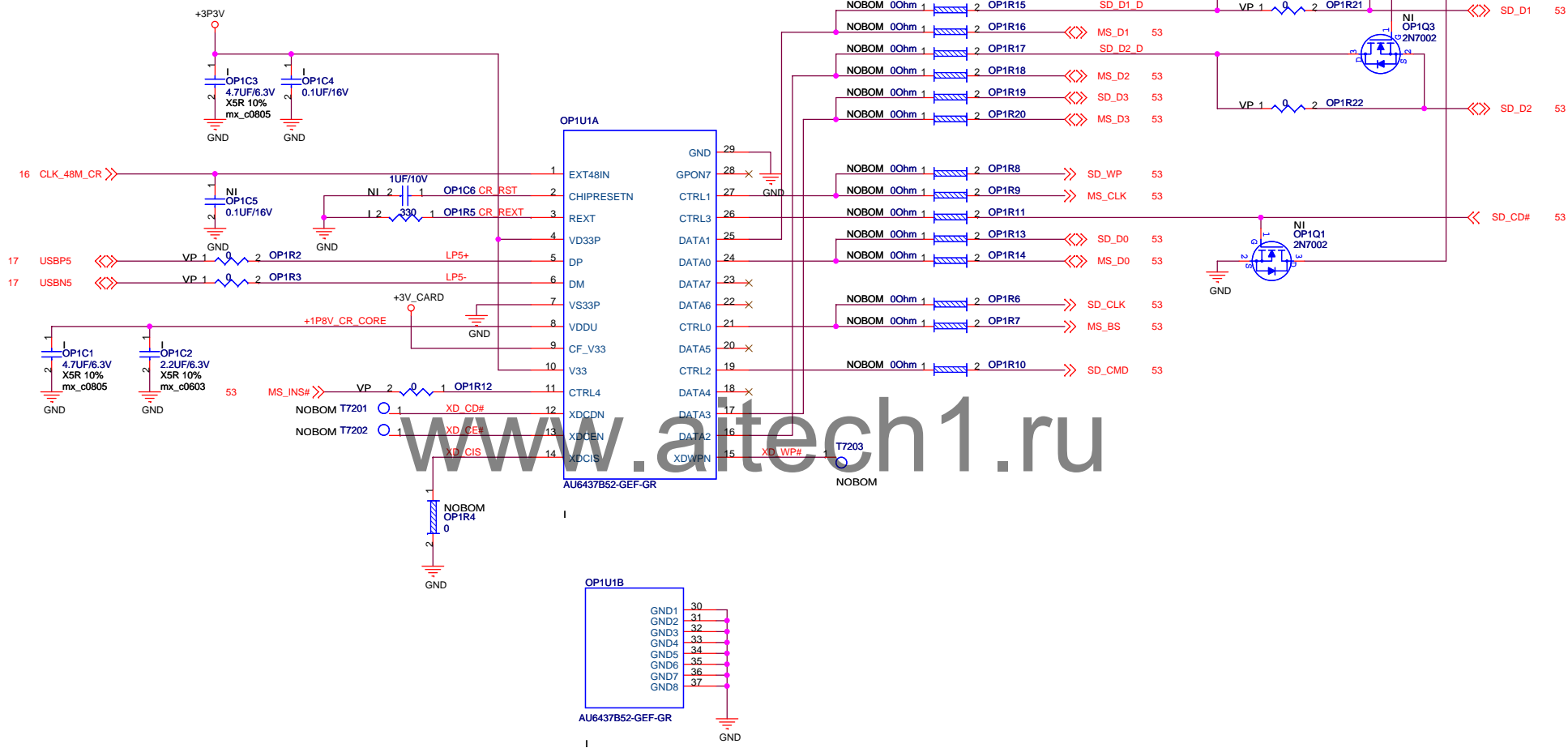
PEGATRON DT-MB RESTRICTED SECRET

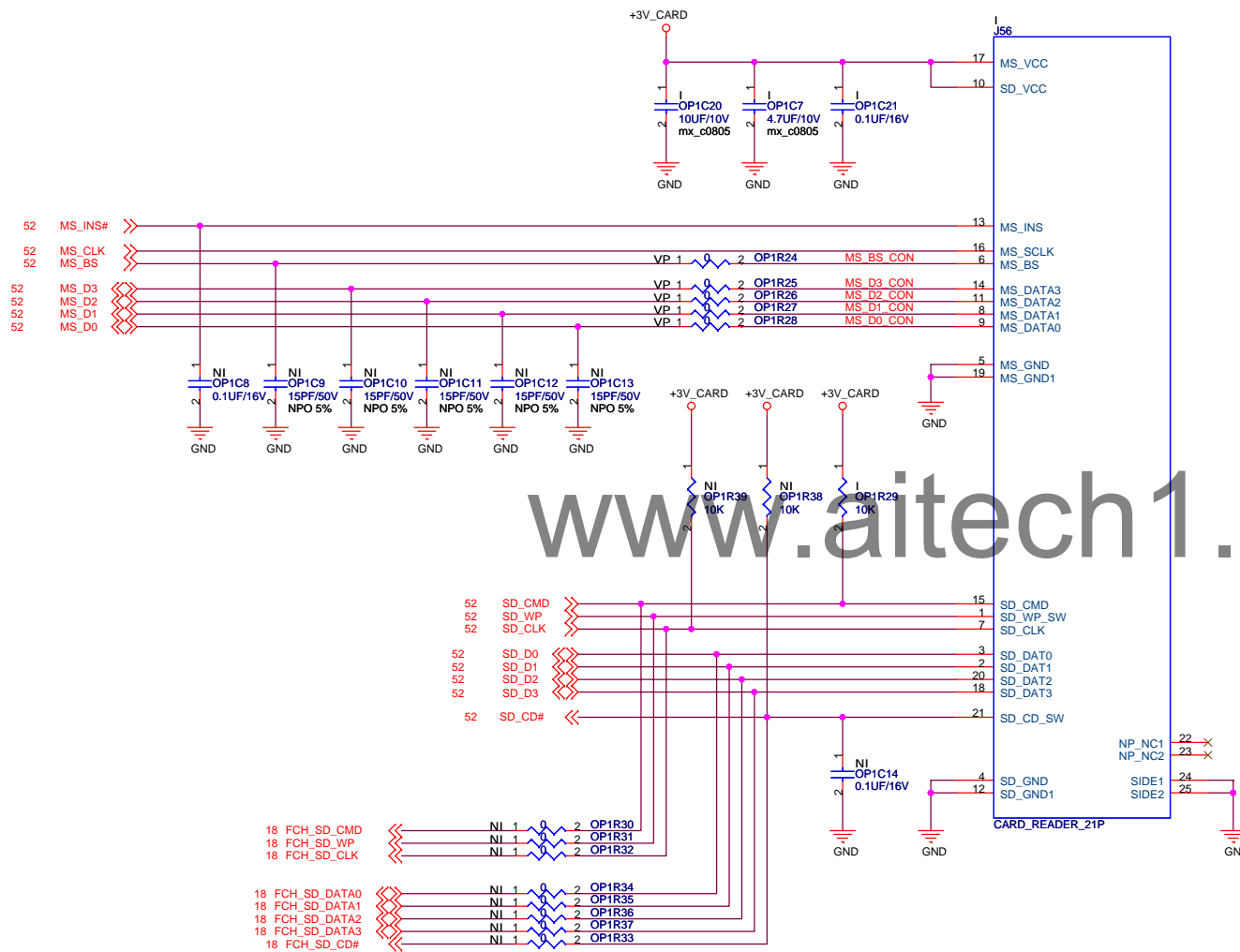
PEGATRON Title : SATA CONNECTOR

Pegatron Corp. Engineer: Shawminger_Ge

Size A3 Project Name AAHD3-AG Rev 1.01

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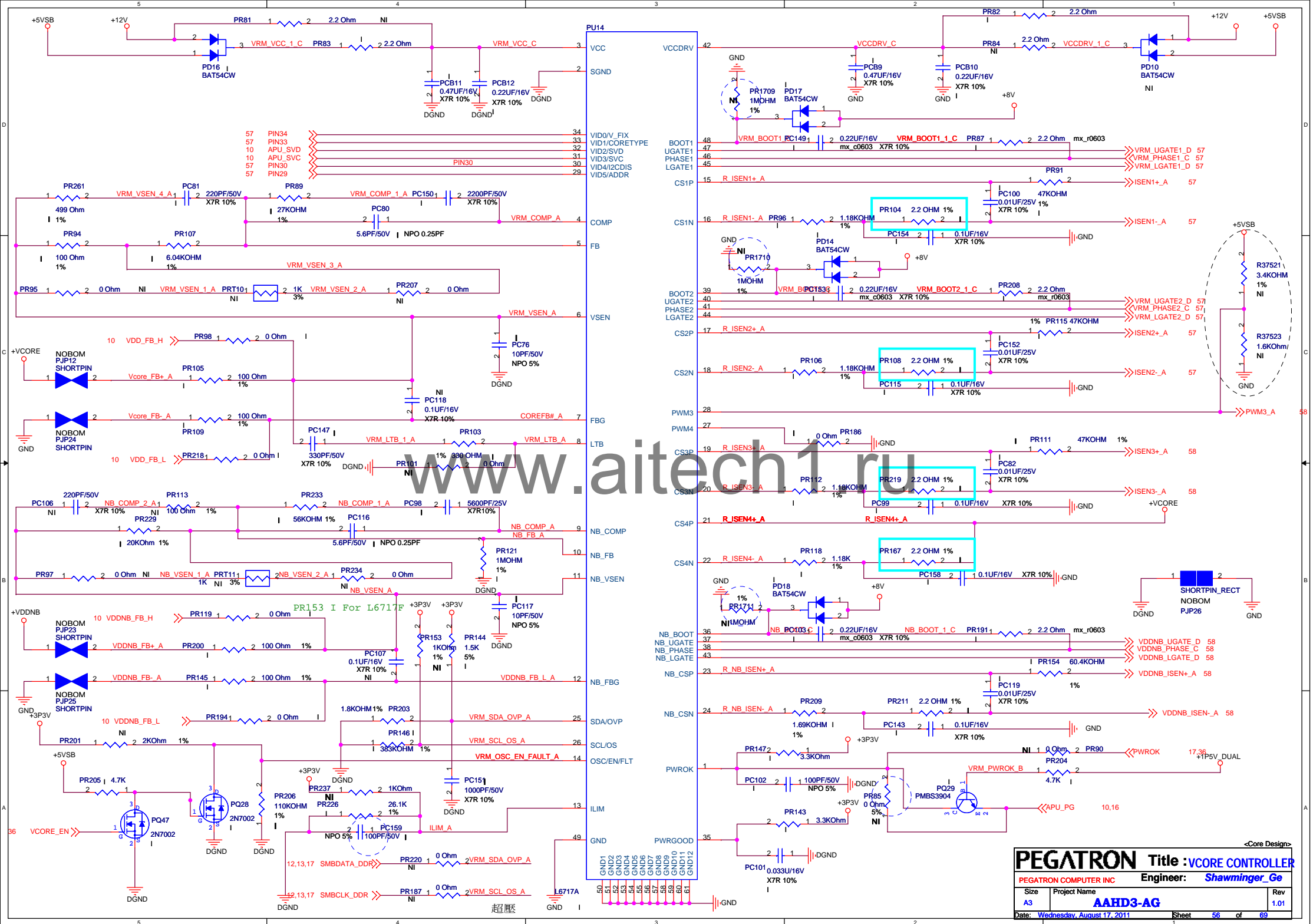


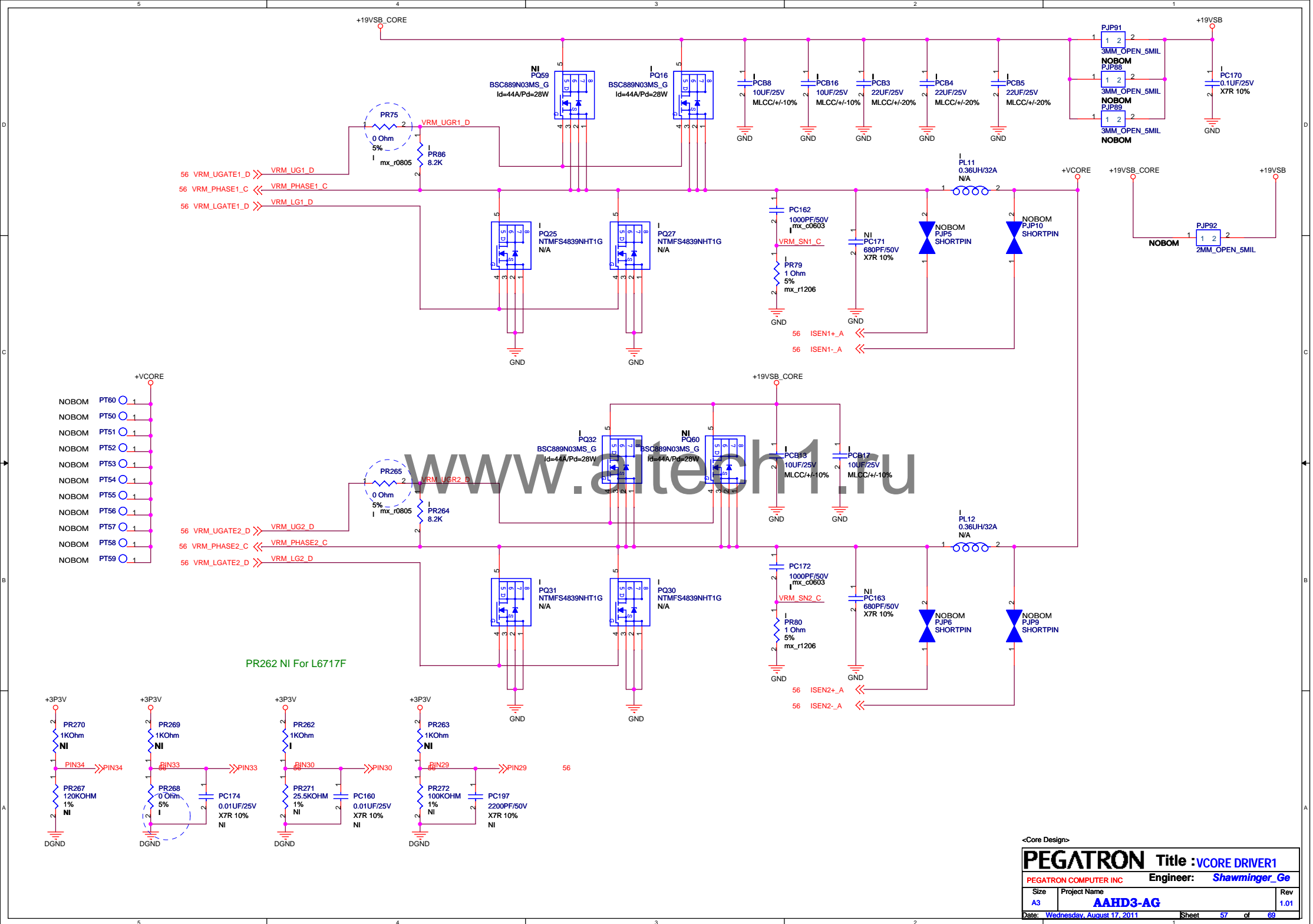


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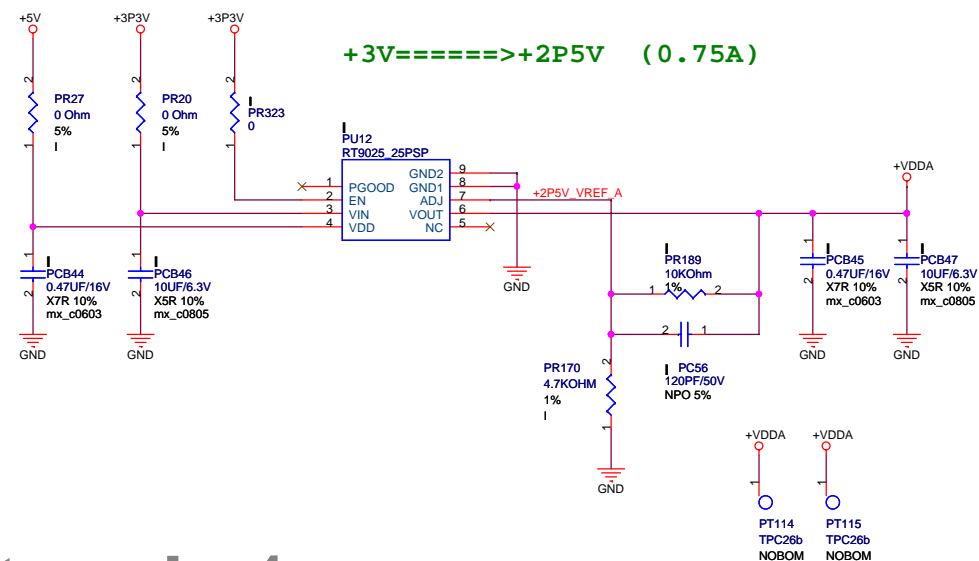
www.aitech1.ru

| | | | |
|----------------------------------|---------------------------------|--------------------------------|-------------|
| <Core Design> | | | |
| PEGATRON | | Title : <Title> | |
| PEGATRON COMPUTER INC | | Engineer: <u>Shawminger_Ge</u> | |
| Size A3 | Project Name AAHD3-AG | | Rev 1.01 |
| Date: Wednesday, August 17, 2011 | Sheet | 54 | of 69 |



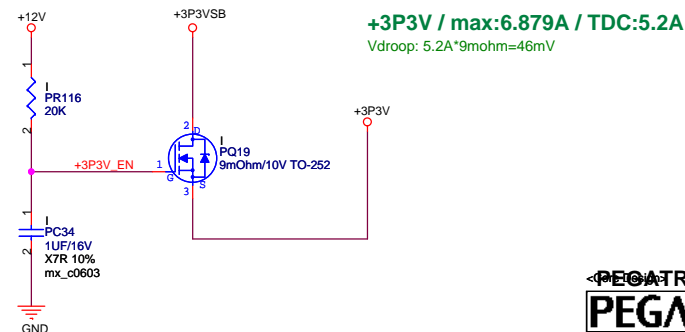




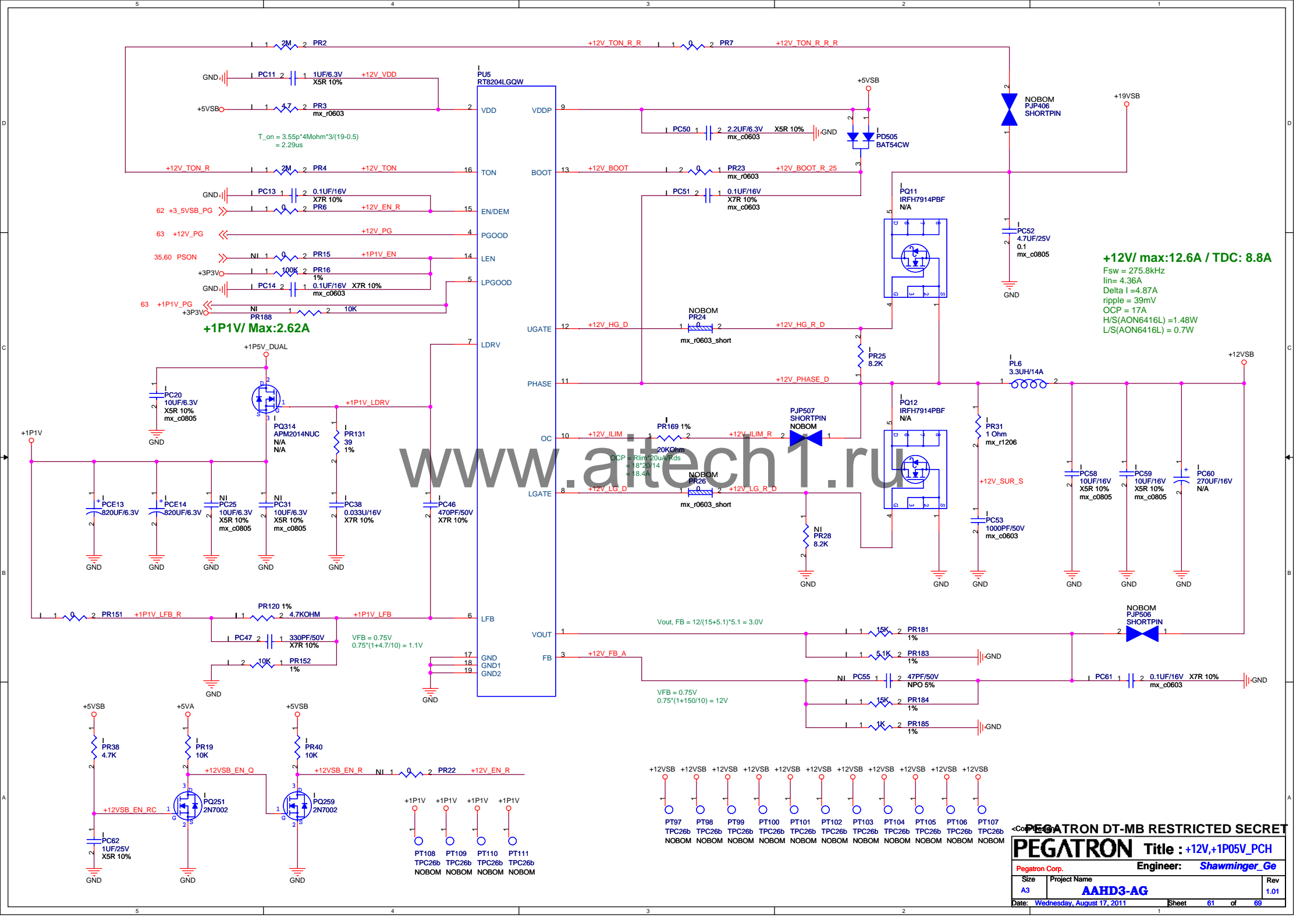


<Core Design>

| | | | |
|--|--|---------------------------------------|------------------------|
| PEGATRON | | Title : +1P1V+1P1V+2P5V | |
| PEGATRON COMPUTER INC | | Engineer: <u>Shawminger_Ge</u> | |
| Size A3 | Project Name AAHD3-AG | Rev 1.01 | |
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$$V_{\text{drop}}: 2.1\text{A} \cdot 0.03\text{ohm} = 0.063\text{V}$$


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+1P1V/ Max:2.62A

+12V/ max:12.6A / TDC: 8.8A
Fsw = 275.8kHz
lin= 4.36A
Delta I =4.87A
ripple = 39mV
OCP = 17A
H/S(AON6416L) =1.48W
L/S(AON6416L) = 0.7W

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| | | | | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| PT97 | PT98 | PT99 | PT100 | PT101 | PT102 | PT103 | PT104 | PT105 | PT106 | PT107 |
| TPC26b | TPC26b | TPC26b | TPC26b | TPC26b | TPC26b | TPC26b | TPC26b | TPC26b | TPC26b | TPC26b |
| NOBOM | NOBOM | NOBOM | NOBOM | NOBOM | NOBOM | NOBOM | NOBOM | NOBOM | NOBOM | NOBOM |

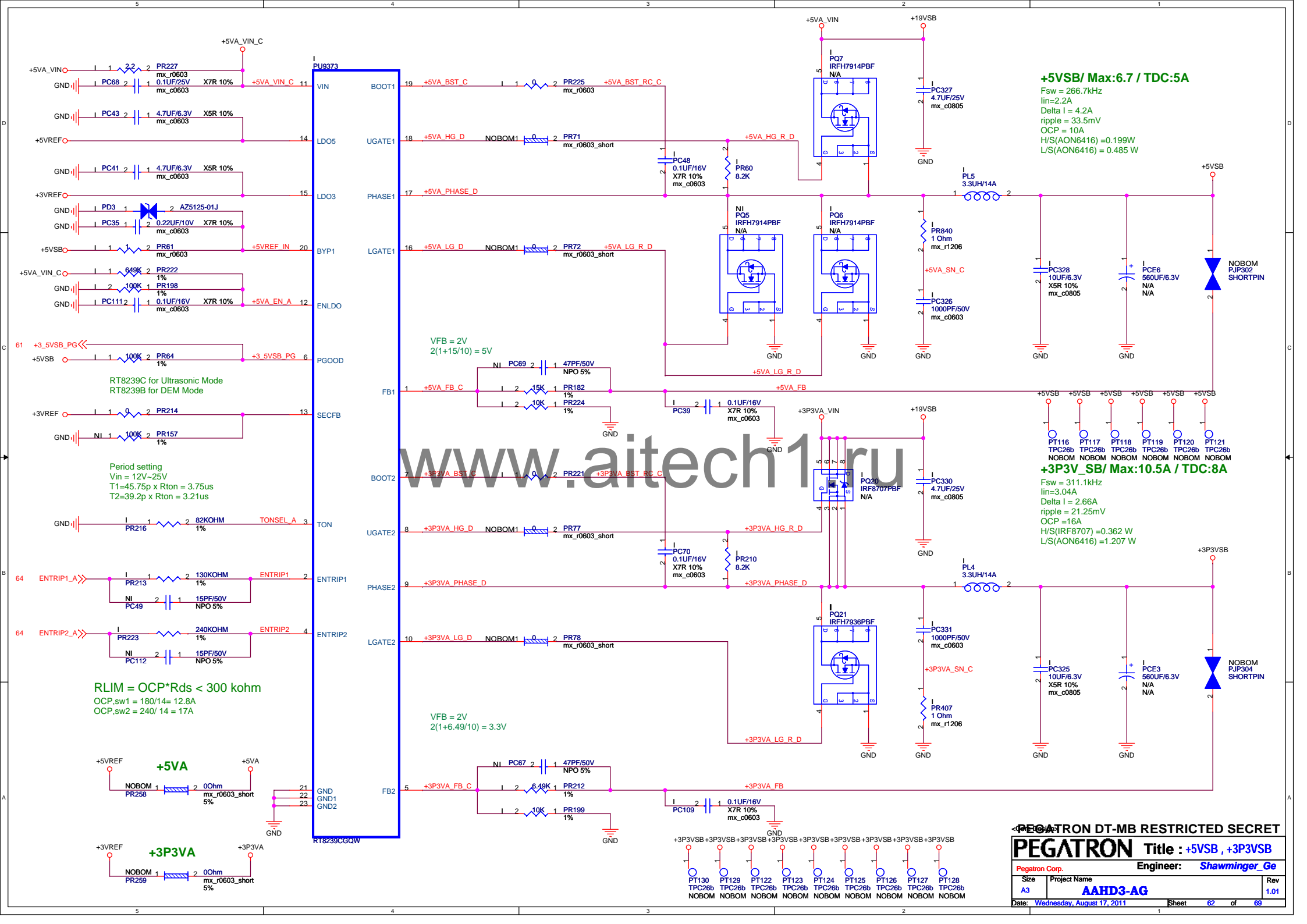
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +12V,+1P05V_PCH

Pegatron Corp. Engineer: Shawminger_Ge

| | | |
|------|--------------|------|
| Size | Project Name | Rev |
| A3 | AAHD3-AG | 1.01 |

Date: Wednesday, August 17, 2011 Sheet 61 of 69



+5VSB/ Max:6.7 / TDC:5A

Fsw = 266.7kHz
lin=2.2A
Delta I = 4.2A
ripple = 33.5mV
OCP = 10A
H/S(AON6416) = 0.199W
L/S(AON6416) = 0.485 W

+3P3V_SB/ Max:10.5A / TDC:8A

Fsw = 311.1kHz
lin=3.04A
Delta I = 2.66A
ripple = 21.25mV
OCP = 16A
H/S(IRF8707) = 0.362 W
L/S(AON6416) = 1.207 W

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +5VSB , +3P3VSB

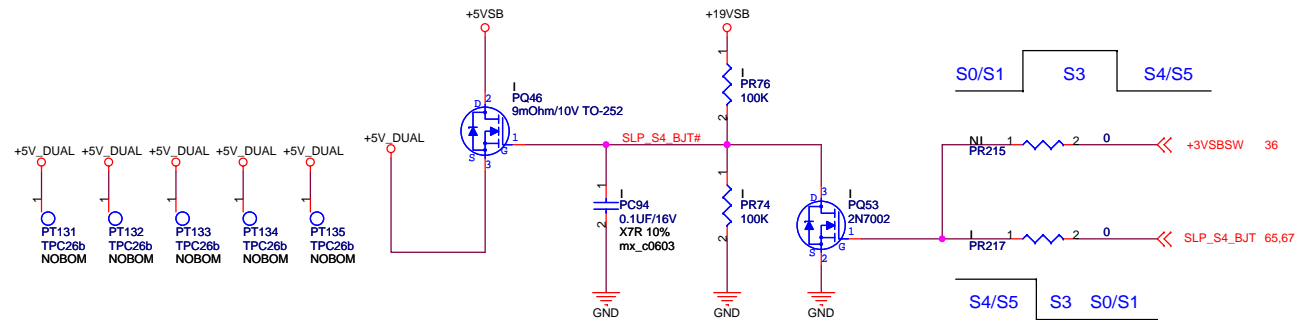
Pegatron Corp. Engineer: Shawminger_Ge

Size A3 Project Name AAHD3-AG

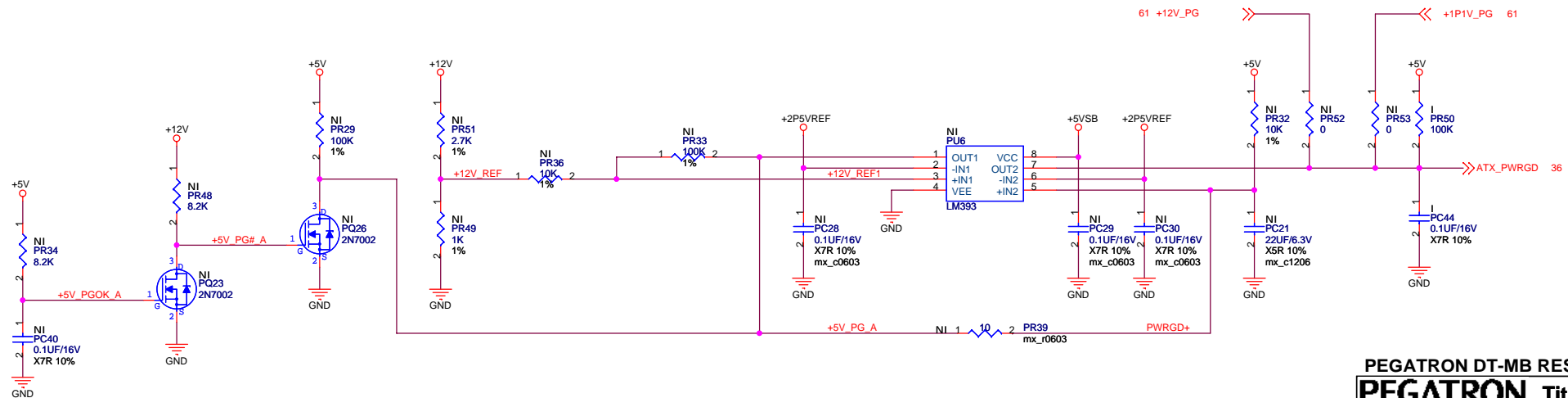
Date: Wednesday, August 17, 2011 Sheet 62 of 69

Rev 1.01

+5V_DUAL /
max:5.3A / TDC:4A
 Vdroop: 4A*9mohm=36mV



ATX_PWRGD



33,36 SIO_CTRL0#

NI PD9 BAT54CW

PR12

PC45 1uF/16V X7R 10% mx_c0603

SLP_SUS_CNTL

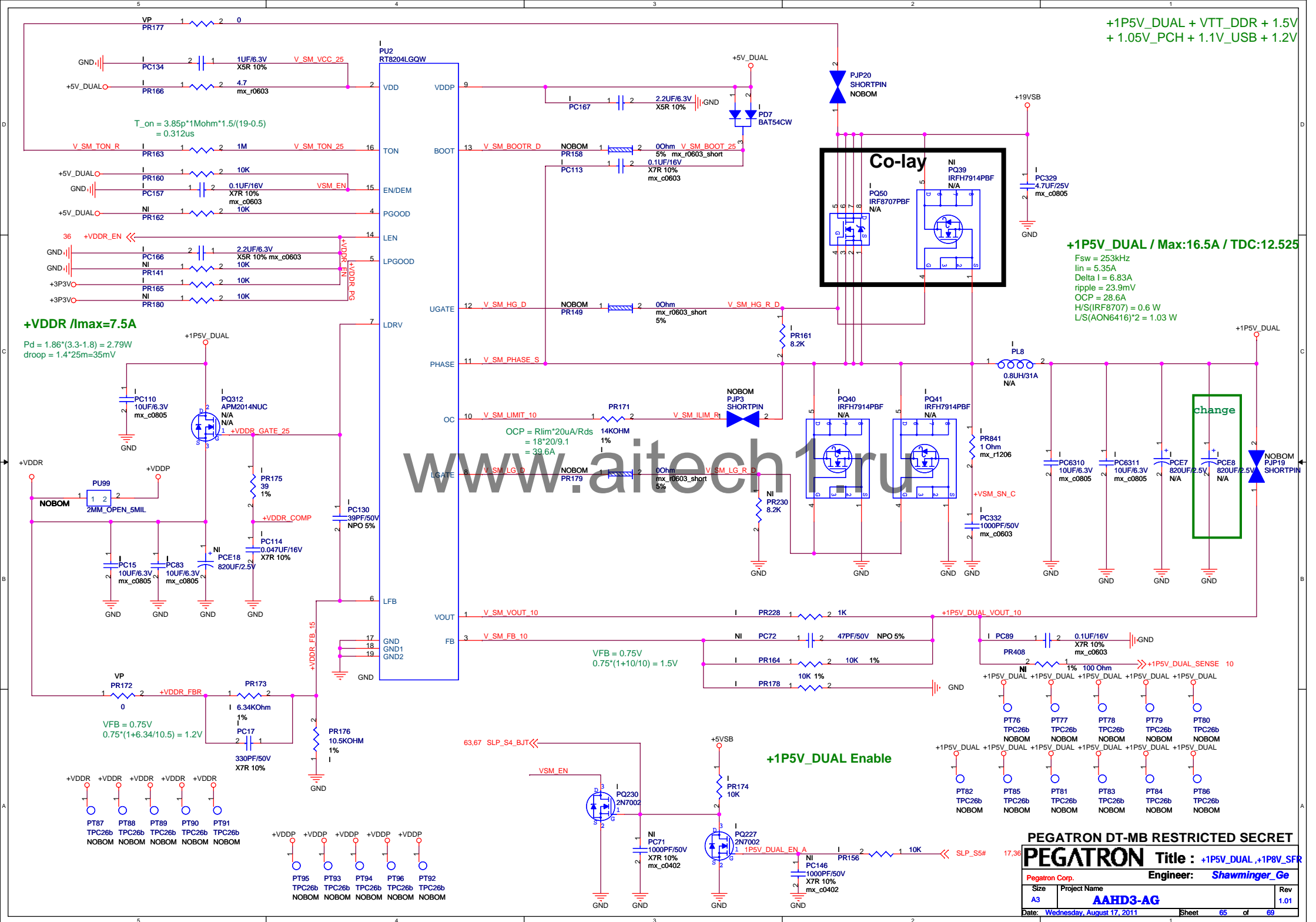
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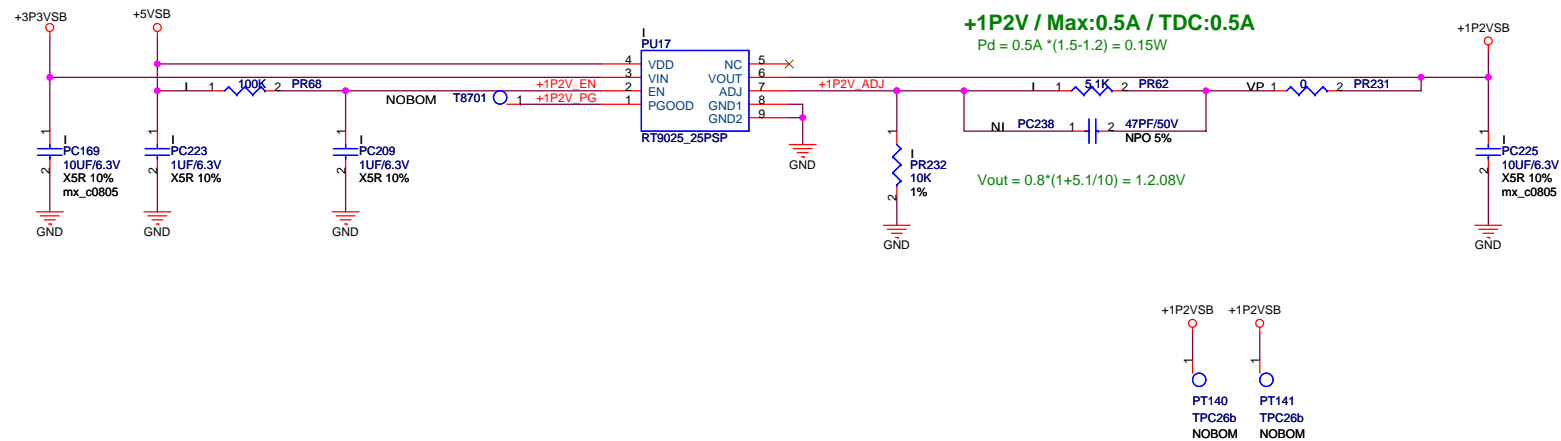
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ENTRIP1_A 62

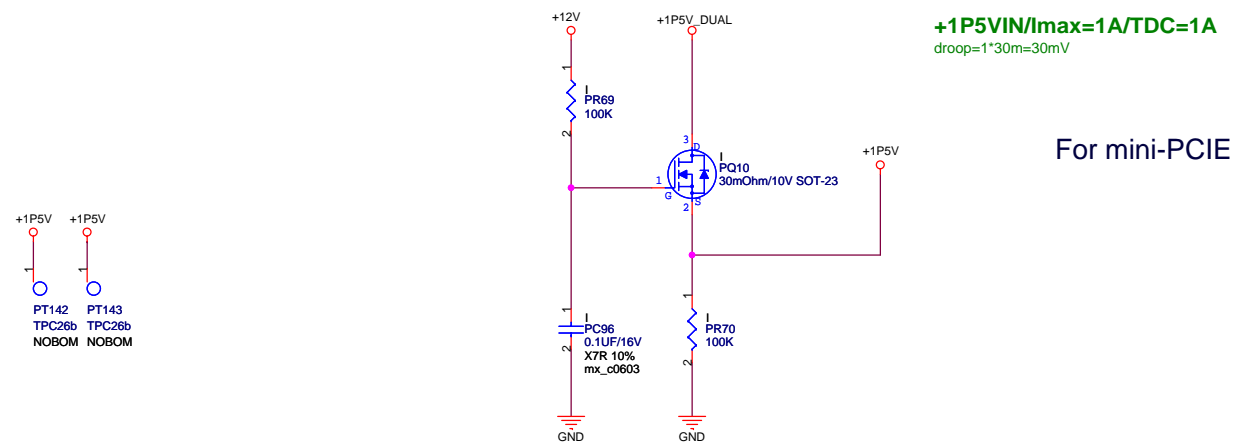
ENTRIP2_A 62

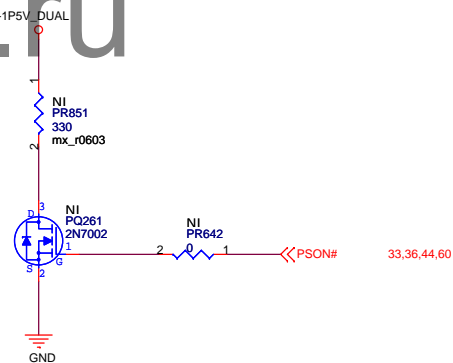
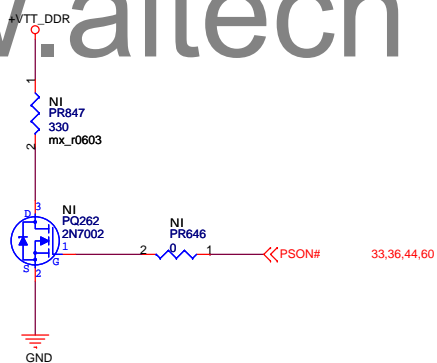
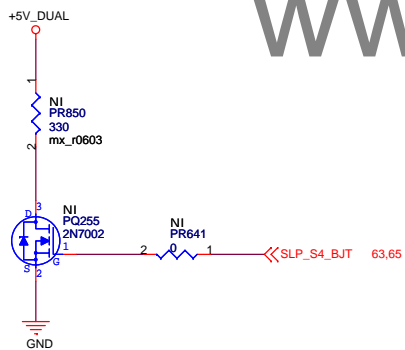
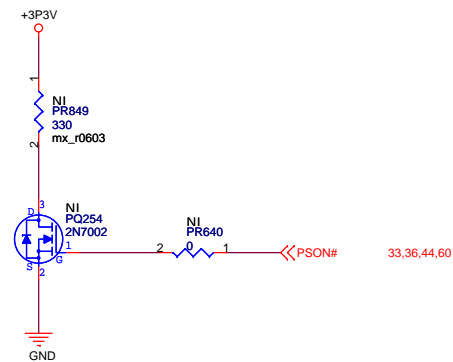
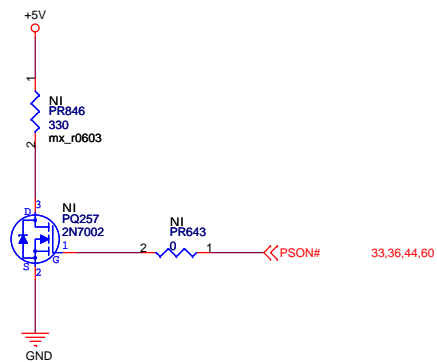
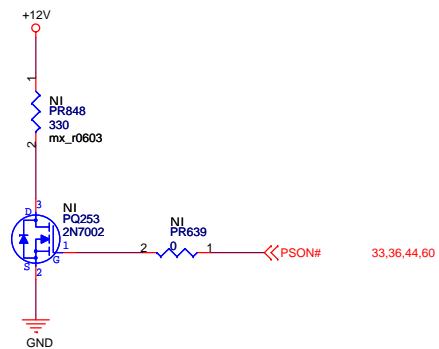
| | | | |
|---|--|--|--|
| <div style="text-align: center;"> SECRET PEGATRON DT-MB RESTRICTED SECRET </div> | | | |
| <div style="text-align: center;"> PEGATRON </div> | | <div style="text-align: center;"> Title : +VTT_DDR </div> | |
| Pegatron Corp. | | Engineer: <i>Shawminger_Ge</i> | |
| Size A3 | Project Name <div style="text-align: center; color: blue;">AAHD3-AG</div> | Rev 1.01 | |
| Date: Wednesday, August 17, 2011 | | Sheet 64 of 69 | |





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